

# 創意專題競賽作品

## 古錐龍舟

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# 構想

- 在想外觀的時候因為端午節快到了所以就把外觀設計成龍舟的樣子。
- 因為我們只有兩個馬達所以設計成龍舟的頭可以前後移動，槳可以划動。

# 程式

```
1 module car_2 (clock, reset, out25ms, out, outch, outend);
2 input clock, reset;
3 output out25ms;
4 output out, outch, outend;
5 wire k;
6 wire [7:0] q;
7 wire [7:0] SW;
8
9 mode555 U1 ( .clock(clock),
10             .reset(reset),
11             .OUT(k)
12             );
13
14 mode225 U2 ( .clock(k),
15             .reset(reset),
16             .q(q),
17             .OUT(out25ms)
18             );
19
20 mode15 U3 ( .clk(k),
21            .reset(reset),
22            .Q(SW)
23            );
24
25 cmp U4 ( .W(SW),
26          .X(q),
27          .OUT(out)
28          );
29
30 decoder3x8 U5 ( .clock(out),
31                .reset(reset),
32                .DEOUT(outch)
33                );
```

Quartus II - C:/altera/91/quartus/car\_2/car\_2 - [mode555.v]

File Edit View Project Assignments Processing Tools Window Help

car\_2

Project Navigator

- Entity
  - Cyclone III: EP3C16F4
    - car\_2
      - mode555:U1
      - mode225:U2
      - mode15:U3
      - cmp:U4
      - decoder3x8:U
      - result:U6
      - Mn:U7

Tasks

Flow: Full Design

Task

- Start Project
- Advisors
- Create Des
- Assign Cor
- Compe D
- Analy
- Fitter
- Assem

```
1 module mode555 (clock, reset, OUT);
2 input clock, reset;
3 output OUT;
4 reg OUT;
5 reg [9:0] q;
6 always@ (negedge reset, posedge clock)
7 begin
8     OUT = q[9];
9     if (!reset);
10        else if (q==10'd554) q<=0;
11           else q<=q+1;
12 end
13 endmodule
```

Messages

Type Message

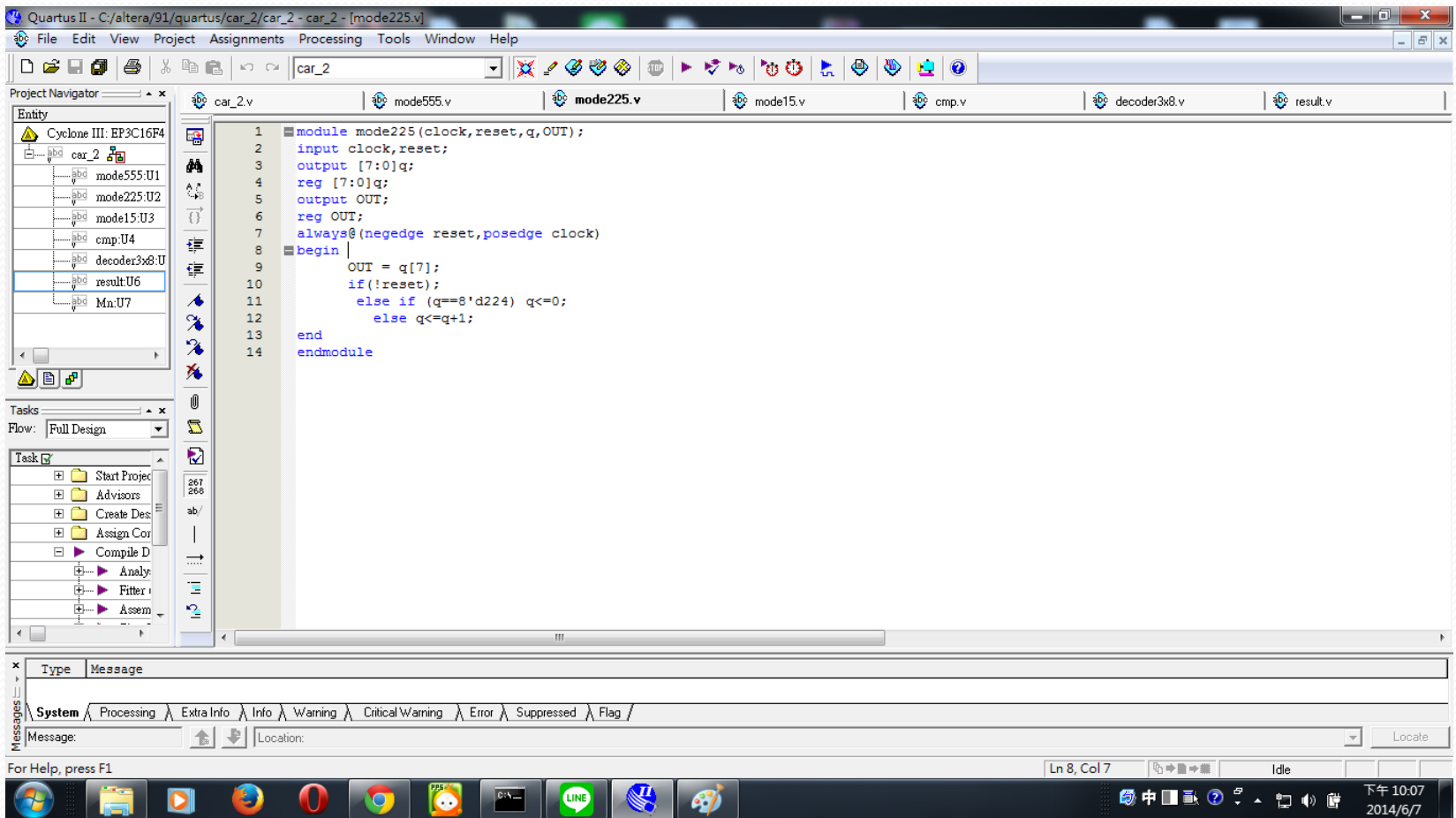
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For Help, press F1

Ln 2, Col 1 Idle

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Quartus II - C:/altera/91/quartus/car\_2/car\_2 - [mode15.v]

File Edit View Project Assignments Processing Tools Window Help

car\_2

Project Navigator

- Entity
  - Cyclone III: EP3C16F4
    - car\_2
      - mode555:U1
      - mode225:U2
      - mode15:U3
      - cmp:U4
      - decoder3x8:U
      - result:U6
      - Mn:U7

Tasks

Flow: Full Design

Task

- Start Project
- Advisors
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- Assign Cor
- Compile D
- Analy
- Fitter
- Assem

```
1 module mode15(clk,reset,Q);
2 input clk,reset;
3 output [7:0]Q;
4 reg [7:0]q;
5 reg [9:0]q;
6
7 always@(negedge reset,posedge clk)
8 begin
9     if (reset==0) q<=9'd0;
10    else
11        if(q==10'd1023) q<=9'd0;
12        else q<=q+1;
13
14 end
15 always@(negedge reset,posedge q[9])
16 begin
17     if (reset==0) Q<=8'd0;
18     else
19         if(Q==8'd180) Q<=8'd0;
20         else Q<=Q+1;
21
22 end
23 endmodule
```

Messages

Type Message

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Ln 5, Col 12 Idle

下午 10:07 2014/6/7

Quartus II - C:/altera/91/quartus/car\_2/car\_2 - car\_2 - [cmp.v]

File Edit View Project Assignments Processing Tools Window Help

car\_2

Project Navigator

- Entity
  - Cyclone III: EP3C16F4
    - car\_2
      - mode555:U1
      - mode225:U2
      - mode15:U3
      - cmp:U4
      - decoder3x8:U
      - result:U6
      - Mn:U7

Tasks

Flow: Full Design

Task

- Start Project
- Advisors
- Create Des
- Assign Cor
- Compe D
- Analy
- Fitter
- Assem

```
1 module cmp (W,X,OUT) ;
2 input [7:0]W;
3 input [7:0]X;
4 output OUT;
5 reg OUT;
6 reg [7:0]W1;
7 always@ (W,X)
8 begin
9     W1 = (W)+8'd45;
10    if (W1>X) OUT=1;
11        else OUT=0;
12 end
13 endmodule |
```

Messages

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Ln 13, Col 11 Idle

下午 10:07 2014/6/7

Quartus II - C:/altera/91/quartus/car\_2/car\_2 - [decoder3x8.v]

File Edit View Project Assignments Processing Tools Window Help

car\_2

Project Navigator

- Entity
  - Cyclone III: EP3C16F4
    - car\_2
      - mode555:U1
      - mode225:U2
      - mode15:U3
      - cmp:U4
      - decoder3x8:U
      - result:U6
      - Mn:U7

Tasks

Flow: Full Design

Task

- Start Project
- Advisors
- Create Des
- Assign Cor
- Compele D
- Analy
- Fitter
- Assem

```
1 module decoder3x8(clock,reset,DEOUT);
2 input clock,reset;
3 output [7:0]DEOUT;
4 reg [7:0]DEOUT;
5 reg [2:0] q;
6
7 always@ (negedge reset,posedge clock)
8 begin
9     if(!reset) q<=0;
10    else q<=q+1;
11 end
12
13 always@ (q)
14 begin
15     case(q)
16         3'd0 : DEOUT = 8'b00000001;
17         3'd1 : DEOUT = 8'b00000010;
18         3'd2 : DEOUT = 8'b00000100;
19         3'd3 : DEOUT = 8'b00001000;
20         3'd4 : DEOUT = 8'b00010000;
21         3'd5 : DEOUT = 8'b00100000;
22         3'd6 : DEOUT = 8'b01000000;
23         default : DEOUT=8'b10000000;
24     endcase
25 end
26 endmodule
```

Type Message

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Ln 8, Col 9 Idle

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Quartus II - C:/altera/91/quartus/car\_2/car\_2 - [result.v]

File Edit View Project Assignments Processing Tools Window Help

car\_2

Project Navigator

- Entity
  - Cyclone III: EP3C16F4
    - car\_2
      - mode555:U1
      - mode225:U2
      - mode15:U3
      - cmp:U4
      - decoder3x8:U
      - result:U6
      - Mn:U7

Tasks

Flow: Full Design

Task

- Start Project
- Advisors
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- Assign Cor
- Compe D
- Analy
- Fitter
- Assem

```
1 module result (x,y,OUT);
2 input x;
3 input [7:0]y;
4 output OUT;
5 reg OUT;
6 always@ (x,y)
7 begin
8     if (y[0]==1&&x==1) OUT=1;
9     else OUT=0;
10 end
11 endmodule
12
```

Messages

Type Message

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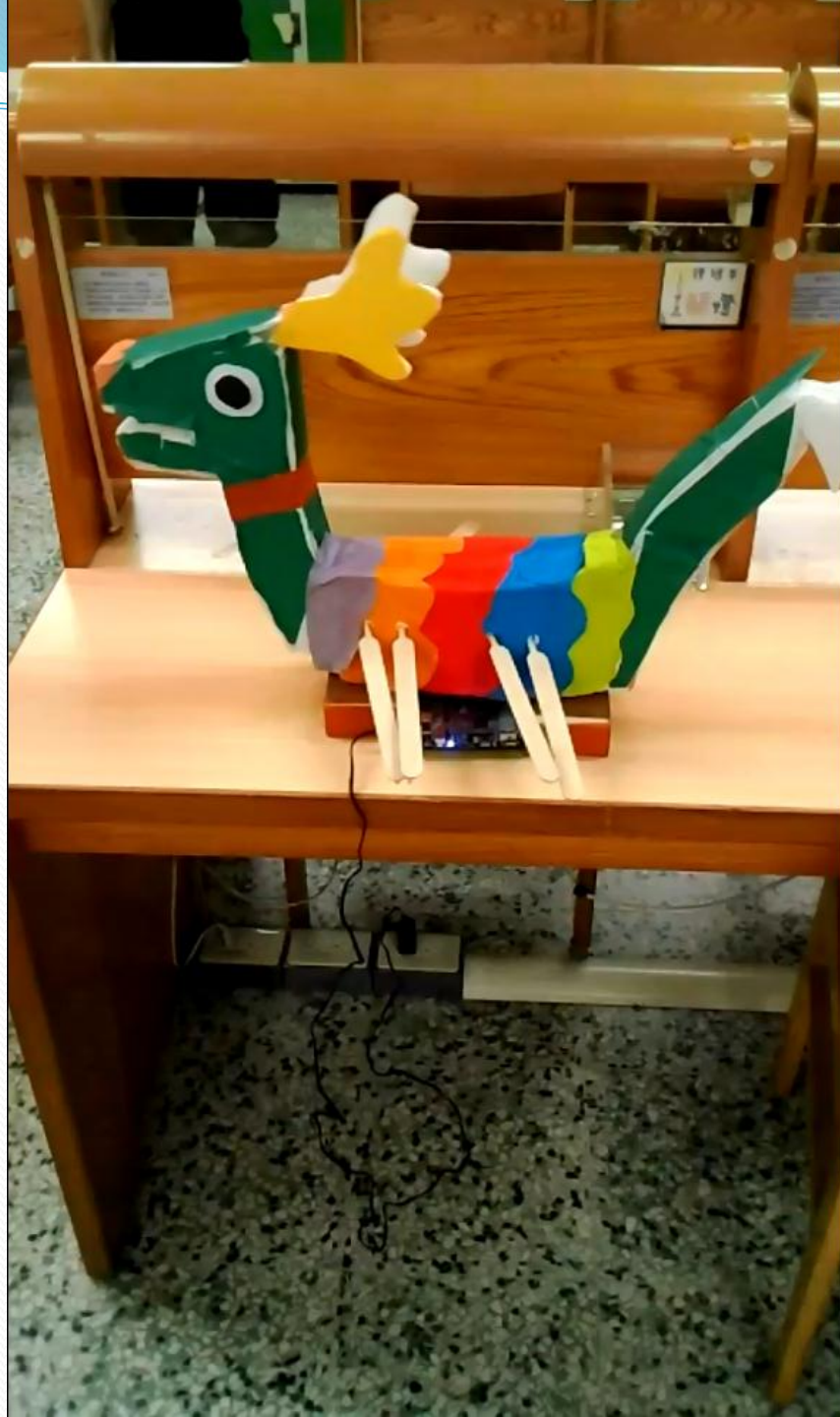
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For Help, press F1

Ln 12, Col 1 Idle

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# 完成圖



# 作品影片網址

- <https://www.youtube.com/watch?v=bINpefmZ3uM>