An integrated dispatching rule with on-line rework consideration in wafer fabrication

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Abstract

In wafer fabrication, the material cost of wafer is expensive. It is imperative to repair the defective wafers produced during the manufacturing process for reducing the cost and increasing the yield of wafer fabrication. However, repairing defective wafer will not only increase the work-in-process (WIP) level but the flow time of rework lots as well. In wafer fabrication, rework of wafer is only allowed in the photolithography area, where is the bottleneck of the entire wafer fab. The purpose of this paper is to develop a dispatching rule concerned with rework for photolithography area.

Keyword：Circuits, Despatch, Manufacturing systems, Modelling, Simulation