行政院國家科學委員會專題研究計畫　成果報告

子計畫五：電子標籤系統晶片之研發(I)

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計畫主持人：田慶誠

計畫參與人員：王志湖　講師

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Abstract

In this paper, a cost effective and simple circuit design for Radio Frequency Identification (RFID) tag is presented. The proposed circuit combines the functions of rectification and modulation to reduce chip complexity and still maintain the function in RFID tag. In the other hand, it minifies the chip size and cost as well. The proposed circuit has been verified by Advanced Design System (ADS) simulations tools and was fabricated in TSMC 0.25um CMOS process.

Measurement and simulation results are presented to verify the design.

Keywords: RFID, TAG, Modulation, Rectification.

摘要

在這篇論文，所要報告的是一個針對射頻辨識(RFID)標籤而言符合成本效益的電路設計，其中所推薦的是一個結合整流及調變功能的新穎式電路，此新穎式電路不僅保持了射頻辨識標籤的完整功能，更縮小了標籤的晶片面積，及降低了成本的花費。本篇論文中，研發電路所採用的模擬軟體為：Advanced Design System (ADS)，及所採用的晶片製程為：TSMC 0.25um CMOS。最後，在此篇論文的結語將電路模擬結果及晶片量測資料互相驗證。

關鍵詞：射頻辨識，標籤，調變，整流。

CONTENTS

I. Intrduction

RFID is hitting the mainstream now for a number of reasons. One of the factors to increasing popularity is that Wal-Mart and
Tesco are mandating that all their suppliers adopt RFID system [1]. According as the tag's ability to read and write data to classify RFID tags. Electronic product code (EPC) has defined five classes, Class0 to Class 4. Each Class has different ability of reading and writing.[2]

RFID tag usually is a battery less portable device. The cost, energy efficiency and the function are the important challenges in the design of RFID circuit. RFID tag has several blocks which has own function to operate. Generally the circuit level main blocks in a tag usually are local oscillator, rectifier, amplitude shift keying (ASK)\On Off Keying (OOK) modulator and demodulator, clock generation, data decoder and encoder. Therefore, to develop cost effective circuits to archive the functions has become a research topic, especially in CMOS technology which makes RFID more competitively. [3]

The cost and chip size are main reason of competition has been mentioned in [4]. The functionality is another guideline in RFID system. But chip size and functionality are trade off for most part. Several methods were proposed to provide solutions to make the function of RFID in CMOS technology. In [5], it dedicated the basic RFID block and circuit. Rectifier block is to generate the DC power supply voltage for front-end circuits. Local oscillator provides the local carrier. Modulator and demodulator are handling the signal with carrier. Power on reset is to generate the chip power on reset (POR) signal. Each distributed block increases the chip size and cost.

In this paper, we proposed the novel RFID circuits which combine regulation and modulation circuit successfully to accomplish chip size and complexity reduction of RFID tag. As mentioned above, the RFID tag (as know as transponder) is a battery less system. All the energy is coupling or transmitting from the reader (as know as interrogator). The proposed rectifier circuit which rectifies the receiving energy from reader can provide a stable dc source on filter capacitor C_{VCC}. After the rectification, the rectifier now can be used as modulator and modulate digital codes into ASK signal for transmission. This circuit can both support internal oscillation carrier or back-scatter modulation schemes. Furthermore, change the LC tank circuit of modulator can cover all bands signal. Such a design maintains lots of functions simultaneously, also increase the competitiveness and design convenience of RFID tag.

II. Purpose

The block diagram of proposed circuit with TSMC 0.25um CMOS process is depicted in Fig. 1. The circuit is comprised of electrostatic discharge (ESD) and back scatting , power on reset (POR) , the rectifier/modulator combining circuit, clock generator, Manchester coder, multiplexer (MUX), Cyclic redundancy check (CRC) coder and timing digital circuit. The generally operating procedures are described as follow.

There are receiving mode and transmitting mode in normal RFID operation. In the receiving mode, antenna of tag receives the RF energy from reader and passes it to rectifier circuit. The rectifier starts to rectify the input carrier with filter capacitor to provide a stable DC source into every block. After obtain the threshold DC voltage, the POR and clock generator provide clock to timing digital circuit. Timing digital circuit operates with CRC coder to generate RFID and CRC codes which will be combined by MUX. Then Manchester coder codes the signal after MUX. Until reader stops sending the carrier, the rectifier will be reused as oscillator and

modulator that modulate the coded signal to ASK\OOK RF signal and transmit through antenna back to reader in the transmitting mode.

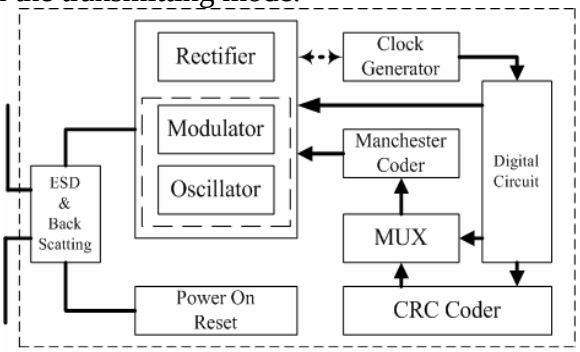

Fig. 1 RFID tag block diagram

III. Research approach

The basic configuration of the proposed rectifier/ modulator circuit is depicted in Fig. 2. It shows the compact design structure of four MOS transistors Q1 to Q4 and will be tested with a external LC tank or antenna. This structure acts as a bridge rectifier in the receiving mode and cross-coupled pair differential oscillator in transmitting mode.

III、A.Rectifier

Fig. 3 shows the topology of rectifier. The LC tank in Fig. 2 is substituted by equivalent ideal transformer with input source. It could represents the antenna of UHF back- scattered type RFID tag or HF loop antenna of magnetic coupled RFID tag. Thus, the proposed tag circuit can be utilized for multiple frequency bands by only changing the tank circuit.

The traditional bridge rectifier circuit is implementing with four diodes. Our new rectifier structure is composed by four MOS transistors. Transistor Q1 and Q2 are PMOS, Q3 and Q4 are NMOS. The circuit operating schemes are described as follows: After antenna receive the energy, during the positive half cycles of the input voltage, Vs is positive, As Vs exceeds V_T (MOS threshold voltage), the Q1 and Q4 begin to turn on and transistor Q2 and Q3 will be cutoff. The charging current is conducted through transistor Q1, capacitor C_{VCC} and transistor Q4. Due to two transistors in series on the conduction path, regulation output voltage Vo of C_{VCC} will be lower than Vs by two transistors V_{DS} drops. The resistor R, shown in Fig. 3, represents the power dissipation on the other digital circuits.

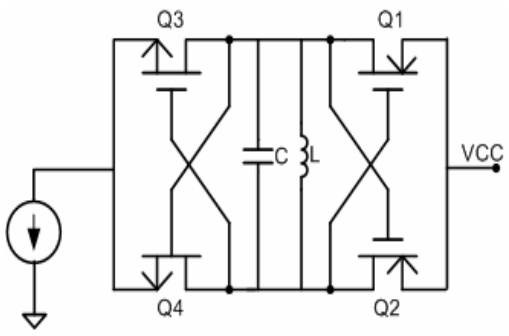

Fig. 2. The basic structure

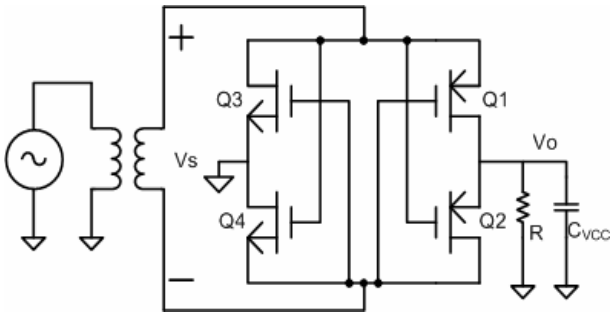

Fig. 3. The rectifier topology

During the negative half cycles of the input voltage, the voltage Vs will be negative. As |Vs| exceeds V_T (MOS threshold voltage), the Q2 and Q3 begin to turn on and transistor Q1 and Q4 will be cutoff. The charging current is conducted through transistor Q2, capacitor C_{VCC} and transistor Q3. Both of the half cycles, current flows through C_{VCC} in the same direction and Vo will always be positive.

However, the transistors, which were turned off, must be able to withstand the peak inverse voltage (PIV) without breakdown. Considering the circuit during positive half cycles, the voltage at source of Q2 is Vo, and the voltage at Drain of Q2 is V_{SD4}. Thus the reverse voltage across Source and Drain of Q2 will be

$$V_{SD2} = Vo - V_{SD4} \qquad (1)$$

V_{SD2} will reach its maximum when Vo is at its peak value of ($Vs_{(PEAK)} - V_{SD1} - V_{DS4}$), so that

$$PIV = Vs_{(PEAK)} - V_{SD1} \qquad (2)$$

For the rectifier shown in Fig. 3, The voltage reduction after rectification, $V_{DS(ON)}$ of transistor, is smaller than traditional diode bridge rectifier. In TSMC 0.25um process, the break down voltage between drain and source is usually great enough to endure PIV in short range tag operation.

Fig. 4 shows the simulation result of rectifier. $V_R(t)$ is the transient rectification voltage on the outer capacitor C_{VCC} Where C_{VCC} is 0.1uF and Vs is 2.9V. There are five response curves due to different CMOS corner models. The output DC voltage is settled to 2.6 V after 30us. Fig. 5 shows the measurement results of rectification. The rising time and regulated voltage is well matched to simulation results.

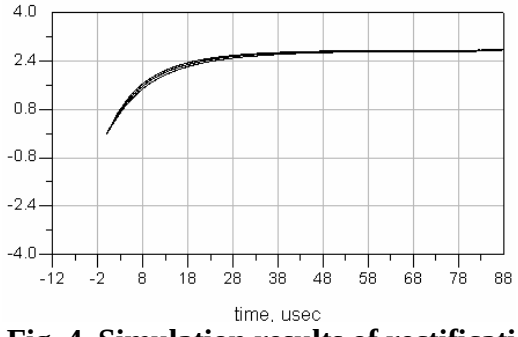

Fig. 4. Simulation results of rectification

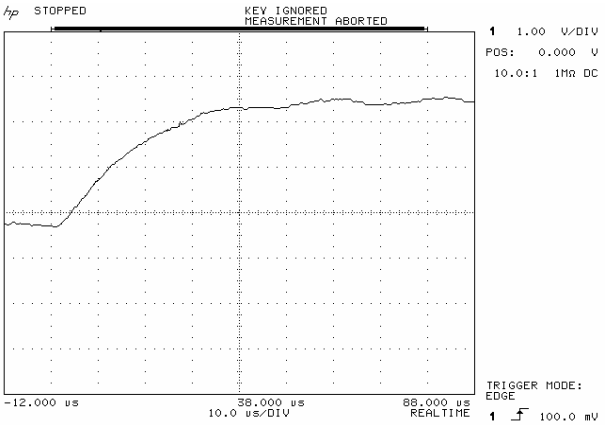

Fig. 5. Measurement result of rectification

III、B.Modulation

In digital communication, the amplitude of ASK\OOK modulation signal is varied according to input coded signal. For the Electronic Product Code (EPC) standard, reader communicates with tags by ASK signal [6]. The modulation index depth minimum is 30% and the maximum is 100%. The modulator structure reused from rectifier is depicted in Fig. 6. The whole structure is base on the circuits of Fig. 2 and Fig. 3 except transistors Q5 and Q6. As mentioned above, this configuration is an cross-coupled pair oscillator originally in the transmitting mode. Transistor Q6 which controlled by timing digital circuit determines whether the tag is in receiving or transmitting mode. Q5 acts as a switch controlled by the output coding signal to form the modulation signal.

The operating procedures of ASK modulation signal are described as follows:

Transistor Q6 is turned on by the digital circuit for transmitting mode. The gate of transistor Q5 is control by the square wave of Manchester coding signal. Transistor Q1, Q2, Q3 and Q4 start to oscillate and generate ASK modulation signal which will be transmitted via the inductor loop antenna. The layout of RFID chip shows in Fig. 7. The size of chip (include pads and digital circuit) is about 1.21mm^2.

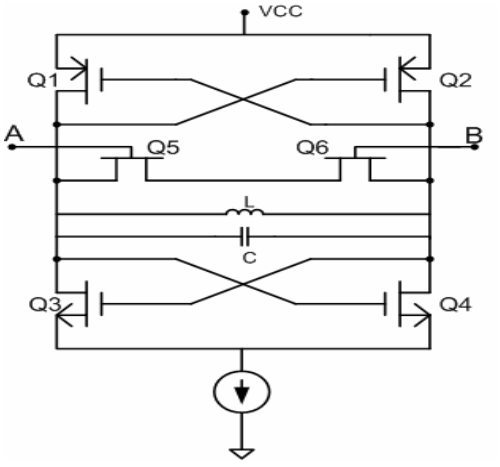

Fig. 6. The modulator structure

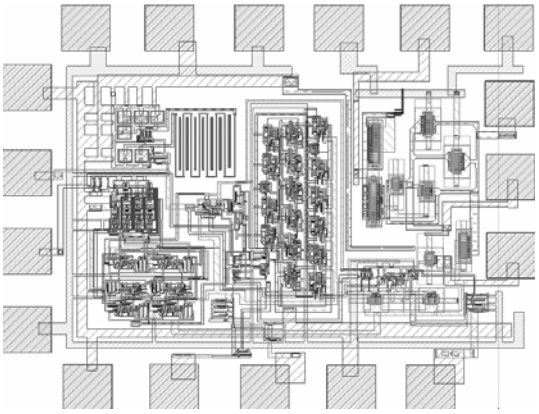

Fig. 7. RFID tag CMOS IC layout

Fig. 8 shows the simulation results of ASK modulation signal. The modulation index controlled by the parasitic series resistance of transistor Q6 and Q5. The square-wave data sequence sending to the gate of Q5 is shown in Fig. 8(a). Fig 8(b) is the ASK modulation signal for transmitting and modulation index is 50%.

All signals of Fig. 8 was measured by Hewlett Packard oscilloscope for transmitting mode. Signal in the Fig. 9(a) is coding by Manchester coder. The different duty cycles of square wave represent 0 and 1 in Manchester coding. Fig. 9(b) is the ASK modulation signal. Fig. 9(c) superimposes digital coding signal and ASK modulation signal. The modulator activated at digital signal rising edge and stopped at falling edge which just verifies and matches the simulation results.

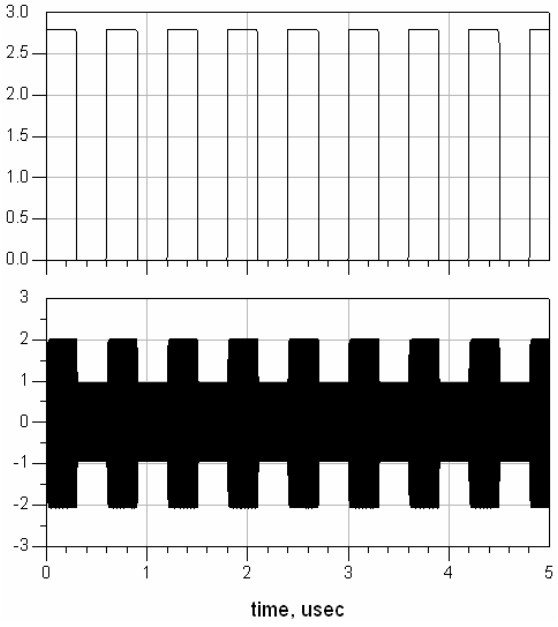

Fig. 8. (a) Data signal of modulation
(b) ASK modulation signal

Table I Specifications of RFID chip

Parameter	Value
Rectification voltage	< 2.8 v
Rectification Charging time	> 35 usec (C_{VCC}= 0.1uF)
Modulation Type	ASK modulation
Cover Rang of frequency	HF, VHF, UHF Band
Rang of Modulation Index	0% ~ 100%

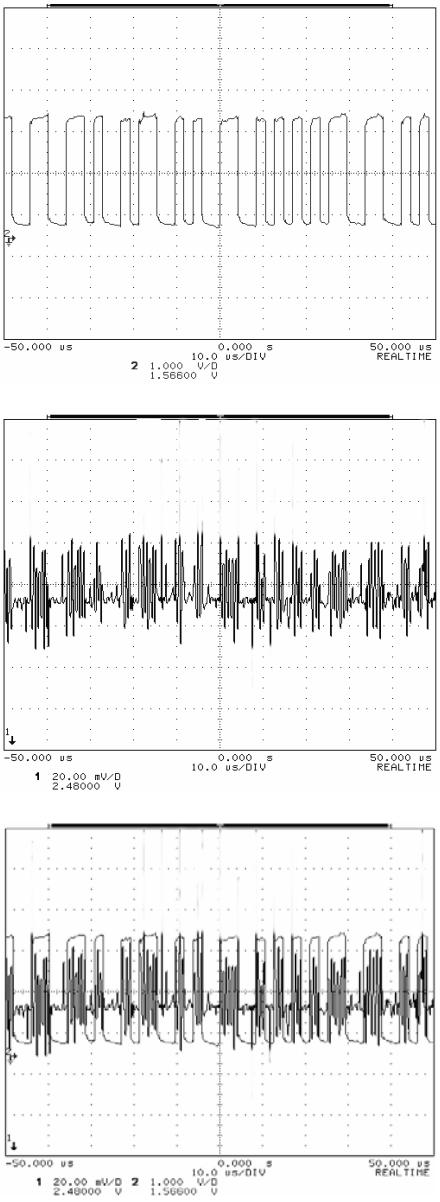

Fig. 9 (a) Digital signal of Manchester coding
(b) ASK Modulation signal
(c)Superimposition of digital and ASK modulation signal

IV. Results and Discuss

The RFID chip is implemented by TSMC 0.25um CMOS process. The digital functions, including POR, clock generator, CRC, MUX, Manchester coding, all worked well. The measured rectification and modulation specifications of RFID chip are listed in table I, which are all matched well to the simulation results.

V. Acknowledgment

The authors would like to thank Nation Science Council (NSC project number : NSC 94-2213- E-216-015) and National Chip Implementation Center(CIC) for technical support. This work is supported by both of these organizations.

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