行政院國家科學委員會專題研究計畫 成果報告

具溫度補償微機電時鐘脈沖產生器
研究成果報告(精簡版)

計 畫 類 別 ：個別型
計 畫 編 號 ：NSC 99-2221-E-216-018-
執 行 期 間 ：99 年 08 月 01 日至 100 年 07 月 31 日
執 行 單 位 ：中華大學通訊工程學系

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報 告 附 件 ：出席國際會議研究心得報告及發表論文

公 開 資 訊 ：本計畫涉及專利或其他智慧財產權，2 年後可公開查詢

中 華 民 國 100 年 12 月 11 日

中 文 摘 要 ： 本計畫研究具有 MEMS 共振器的時鐘脈沖產生器，振動式共振子的結構採單臂懸吊式設計，利用 TSMC 所提供的 CMOS 微機電製程最上層的金屬當兩電極及共振子，利用乾式蝕刻製作。其共振頻率與懸臂長度、寬度、及厚度及與電極的間隙有關，將利用 ANSYS 從事力學模擬，中心頻率先定在最常見的 10MHz，並由此求出電氣參數，再利用參數萃取法求出等效電路，作為下階段 IC 設計的參考。MEMS 的等效電路為串聯 Rm、Lm、Cm 再並聯 Co 電容，反應兩電極的寄生電容。此共振器先單獨製作測試，俟測試良好之後用 Bond wire 與 CMOS 交叉耦合對主振器連接，做完整振盪器溫度測試，以確定溫度係數。最後再設計具有溫度補償功能及振動子擺幅控制的全積體化電路。本計劃 CMOS 振盪器的性能，電流約 20mA，電源電壓為 3.3V，測試載具體積為 5*3.2*0.85mm，中心頻率為 10MHz，相位雜訊為-70dBc@10KHz，頻率偏差及穩定度約 100ppm。

中文關鍵詞： 微機電、振動式共振子、單臂懸吊、交叉耦合對、時鐘脈沖

英 文 摘 要 ： This project studies the clock oscillator with MEMS vibrating resonator. The resonator is built by a cantilever structure, which is formed by the top metal layer in TSMC CMOS process. Two electrodes and the resonator are separated via dry etching proposed by CIC. The center frequency of the resonator determined by the length, width, and thickness of the cantilever is examined by the three-dimensional software ANSYS. After that, the electric performance is obtained and is translated in an equivalent circuit, which is employed in the integrated circuit simulations. The temperature coefficient of the resonator is studied by oscillator with the resonator bonded to the CMOS cross-coupled pair. With this information, a total integrated MEMS oscillator is developed. The performances are aimed to 20mA current consumption, power supply 3.3V,in package size 5*3.2*0.85mm. The center is designed at 10MHz with phase noise at 10KHz offset is -70dBc. The frequency stability in within 100ppm.

英文關鍵詞： MEMS、MicroElectromechanical、 Cantilever、Cross-Coupled Pair，Clock Oscillator

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計畫主持人：高曜煌
共同主持人：
計畫參與人員：

成果報告類型(依經費核定清單規定繳交)：■精簡報告　□完整報告

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中　華　民　國 100 年 7 月 31 日

Balanced SAW Oscillators with Cross-Coupled CMOS Pair

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***Abstract* — The cross-coupled pairs in CMOS are employed to the voltage controlled oscillator with surface acoustic wave (SAW) resonator. The problem of latch, which is not encounted in conventional LC oscillator, is essential in our case. With a careful design in bias this problem is solved. This oscillator has the advantage of inherent opposite polarity appeared on the terminals of SAW resonator, which leads to fast growing amplitude during transition. As compared to the well known Colpitts oscillator, the transition period is significantly shrinked. For completeness three kinds of oscillator with single ended, balanced Colpitts, and cross coupled one are compared in terms of figure of merit (FOM) under the same magnitude across the resonator. Also the power consumption and phase noise are indicated.**

I. Introduction

Clock oscillators utilize the high quality factor piezoelectric resonators to obtain the stable frequency. As the author's knowledge, the configuration of the oscillator normally adopt the Pierce or Colpitts oscillators with single ended output [1]. As the clock frequency is raised The outputs are normally converted to a differential pair before connected to next stages, such as mixer in receiver and counter or phase detector in phase locked loop to take advantages of noise free and direct match to the inputs of preceded stages. Although the configurations of cross coupled pair are effective in the rf oscillators with parallel LC tank [2-6]. They are not yet applied to the oscillators with piezoelectric resonator. The key factor lies in the property of dc insulation in the piezoelectric resonator. In LC resonator, the metal-wounded inductor not only provides the ac inductance but also provides the dc short circuit between two drains such that the latch phenomena often seen in the cross pair is automatically suppressed. As applied to the piezoelectric resonator, the pair already goes into latch situation as a memory cell in the digital circuit. In this study we try to use this compact cross-coupled pair to construct a voltage controlled oscillator with surface acoustic wave resonator (SAW), which is denoted as VCSO and intended to use in the clock and data recovery (CDR) shown in Fig. 1. A simple method of biasing is proposed to overcome the latch problem. The phase noise and transition time are especially investigated. Due to the manufacture variation and temperature, Tuning capability is needed to overcome the frequency precision. Here, two switched capacitances are designed to increase the tuning range. Low power consumption under TSMC 0.18um CMOS process is implemented. In the meantime, a comparison in performances with other balanced type of Colpitts is presented [7, 8].

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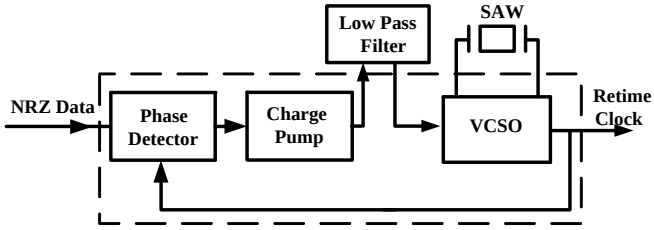

Fig. 1 Application of VCSO in giga-bit CDR

II. Oscillator with Differential Outputs

SAW resonator exhibits a series LC resonance in parallel with a capacitance regarding to motional vibration and parasitic of interdigital electrodes, respectively. The equivalent circuit parameters of SAW resonator are listed in Table I. Co is the parasitic capacitance of interdigital transducer. Ls, Cs, and Rs are the series equivalent circuit of the piezoelectric motion. As applied to oscillator, two operating modes of series and parallel are often employed. The former has the resonator acted in series short circuit, while the latter acts as parallel open circuit at resonance. Here, the latter is utilized. The schematic of VCSO is shown in Fig. 2a. Two stacks in CMOS process are used for low voltage operation. As usual, the cross-coupled nMOS pair provides the loop gain and 2π phase to satisfy the so called Barkhausen's condition. The drain voltage from the left nMOS M5 is fed to the gate of the right one M6. Then the drain voltage of M6 returns to the gate of M5. It is noted that, due to the insulated nature of SAW resonator, the cross coupled nMOS are actually latched. To avoid latching, two small dc blocking capacitors C_1 and C_2(=0.9pF) are inserted into the signal paths to block the latching. In the meantime, the gates of the active nMOS's are connected from two duplicated current mirrors, which allow the same dc bias but with opposite ac swing. With such an arrangement, the latch problem can be easily overcome.

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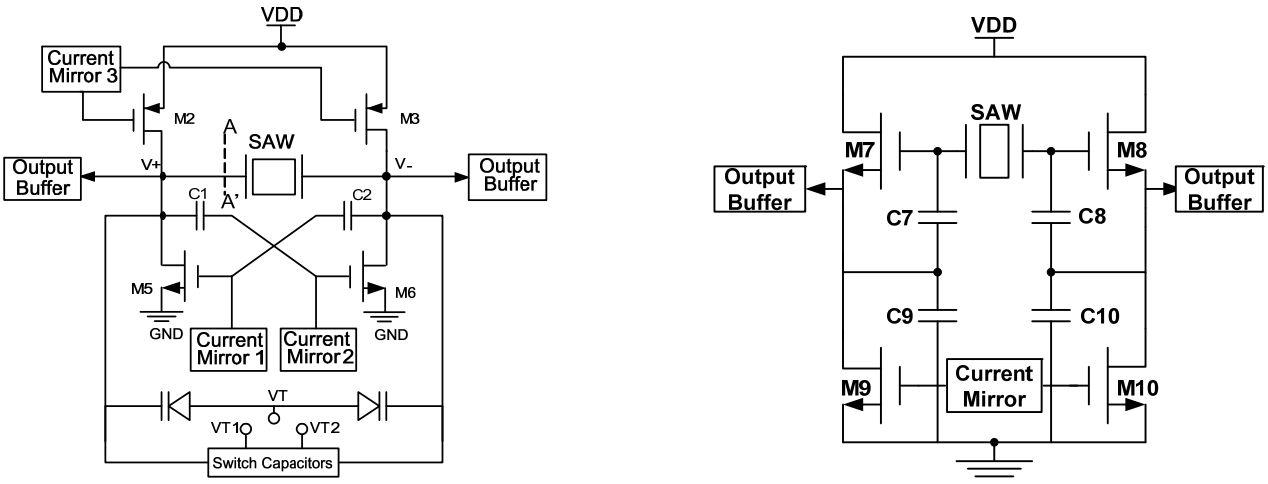


Fig. 2 (a) Schematic of the balanced oscillator with cross-coupled CMOS pair and (b) Balanced Colpitts oscillator.

To test the occurrence of oscillation, the impedance seen at the intersection plane of A_A' indicated in Fig. 2a is examined. During calculation the A-A' is disconnected without disturbing the dc bias. A small ac voltage source is inserted and the input impedance is then calculated by measuring the current. The oscillation starts as long as the real part of impedance is negative and imaginary part crosses the zero axis with positive slope. Both conditions are also equivalent to the Barkhausen's conditions. The design factors have C_1, C_2 size, MOS dimension, size of switching capacitance, and varactor size. Capacitance C_1, C_2 are traded off in area and negative resistance. MOS dimensions are traded off is between phase noise and tuning. Phase noise gets better as MOS area is enlarged. However, its parasitic degrades the tuning capability. The parameters of transistors are extracted from TSMC 0.18um CMOS process. The aspect ratio of M2 and M5 are 60/.18 and 30/.18, respectively. The current consumption in the core is 2,68mA. The effects of bonding wire and pads are also taken into account. The results by using microwave software ADS is shown in Fig. 3. The starting frequency is determined from the zero crossing point of the imaginary part, which is equal to 425.1MHz as denoted M8.

Table I Parameters of 425MHz SAW Resonator

Co	Rs	Ls	Cs
3.8pF	10.53Ω	46.3uH	3.03fF

For clearance, the capability of the balanced Colpitts oscillator as shown in Fig. 2b is also examined. It is basically built from two single-ended Colpitts oscillator sharing one SAW resonator. M7 and M8 are the main amplifiers and M9 and M10 are the current sources. For comparison, a single ended Colpitts with similar model is firstly constructed. One pin of the resonator is connected to ground. With this success, the balanced one is easily obtained just by copying the single ended one and connecting the resonator to the gates of the main amplifiers. The SAW resonator now is re-modeled as two series resonators with center point virtually grounded [7, 8]. The ac swing across the SAW resonator in each oscillator is set equal to 100mV by trimming the aspect ratio of the transistors. The current consumptions of the core circuit without buffer are listed in Table II. Die size and phase noise are also indicated. It reveals that output power and turn-on transition in cross-coupled oscillator are the best. The turn-on transitions in cross-coupled pair and single-ended Colpitts are shown in Fig. 4. The former is about 150us in Fig. 4a and the latter is about 500us in Fig. 4b. The Balanced Colpitts is the worst. Because no strong force exists to identify the polarity, the transition period may take a long time. According to our observation, it takes about 5ms (not shown here). The cross coupled one as expected has the shorted transition time.

Phase noise is medium. The single-ended one has the best about -159.2dBc at 1Mhz offset. It seems to be due to just only one active transistor. As for the high power consumption in balanced Colpitts is due to the doubling in equivalent Co capacitance, which degrades the negative resistance.

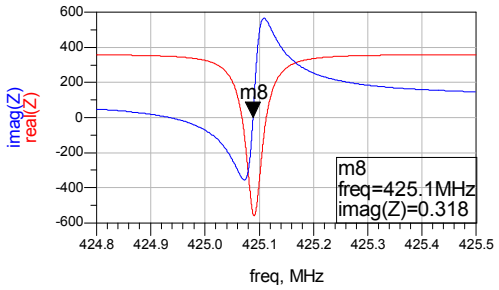


Fig. 3 The calculated negative resistance and reactance

To compare the performances, figure of merit is often used as

Table II Predicted Performances

	Cross-couple	SE Colpitts	Balanced Colpitts
CMOS Process	0.18um	0.18um	0.18um
Power Supply (V)	1.6	1.6	1.6
Current (mA) (no Buf)	3.05	1.27	5.22
Power Dissipation (mW) (no Buf)	4.88	2.032	8.352
Oscillator Frequency (MHz)	622	622	622
Phase Noise (dBC/Hz@1MHz)	-156.6	-159.282	-154.309
Output Power (dBm)	2.94	-9.725	-9.942
Transition (usec)	150	500	5000
FOM	205.6	212	200.9

$$FOM\,(dB) = 10\log\left[\left(\frac{\omega_o}{\Delta\omega}\right)^2 \frac{1}{L(\Delta\omega)\times P}\right]$$

where P is the power consumption of the core circuit, $\Delta\omega$ is the offset angular frequency from the carrier, ω_o is the center frequency, and L(Δω) is the phase noise. It reveals the cross coupled one is better than balanced Colpitts.

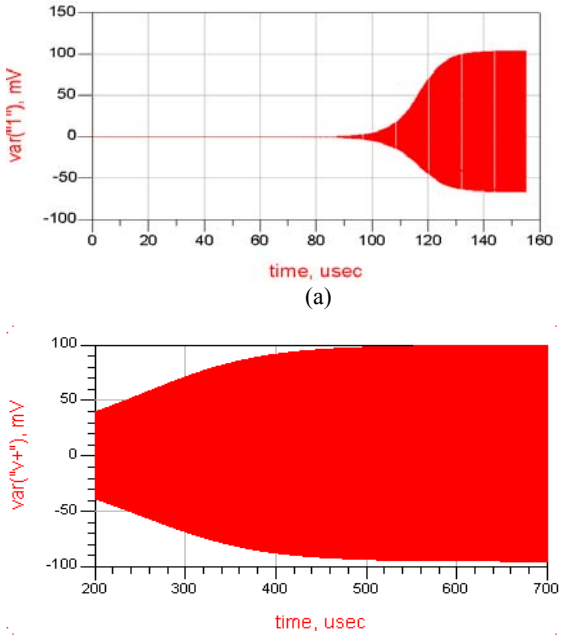


Fig. 4 Transition period in (a) cross-coupled pair and (b) single ended Colpitts oscillators.

III. Performances

The layout is illustrated in Fig. 5 with die area about 0.545×0.510mm^2. The chip is fabricated by TSMC. The measured results are shown in Fig. 6. The differential waveform with p-p 250mV is demonstrated in Fig. 6(a). The low phase noise with high quality factor SAW resonator is demonstrated in Fig. 6(b). The slope near the carrier appears 1/f^3 with noise floor around -160dBc. The continuous tuning range as shown in Fig. 6(c) is around 30ppm, depending on the size of MOS varactor, which is varied from 1.8pF to 2.45pF with VT from 0 to 1.8V. Two tuning switches are also added to increase the application. Capacitances in VT1 and VT2 switches are 0.1pF and 0.3pF, respectively.

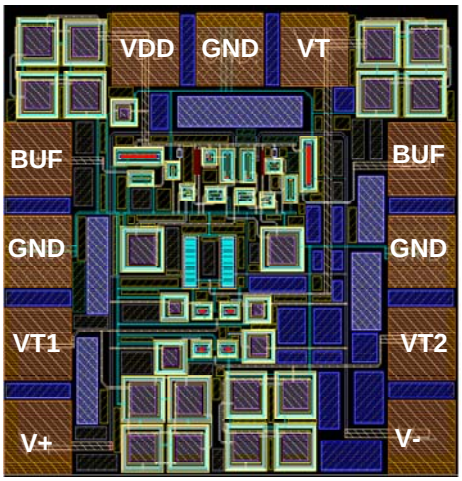


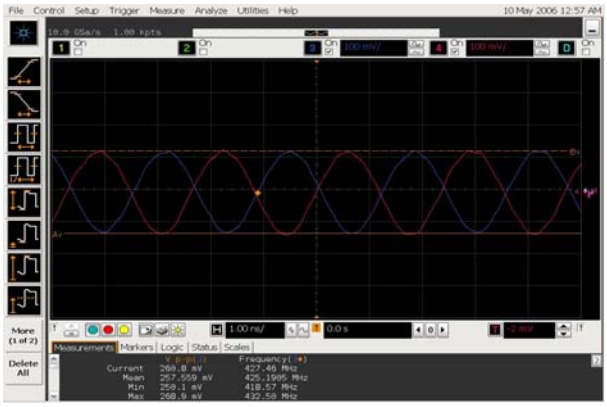
Fig. 5 Layout of the cross coupled SAW oscillator

VI. Conclusion

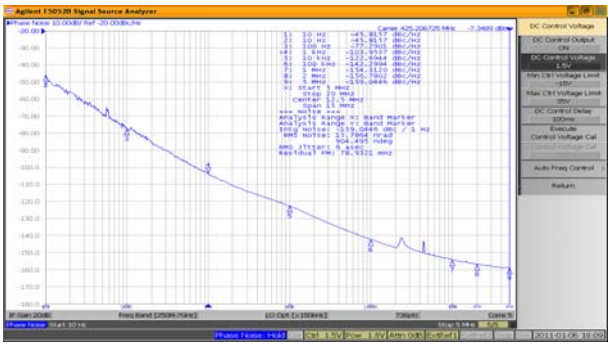
In this study a balanced VCSO using the compact cross coupled configuration is first presented. The latched problem is solved by separating carefully the drain and gate voltages. The SAW resonator acts as a parallel tank circuit to select the desired frequency. The nature of inverse polarity between gate and drain drives quickly the oscillator into steady state as compared to the balanced Colpitts one. The tuning range in this version needs to be improved in the future. Our results can be extended to other high frequency and high Q resonators such as MEMS and FBAR.

ACKNOWLEDGEMENT

The authors would like to thank National Chip Implementation Center and National Science Council, Taiwan, R.O.C., for chip implementation and financial support.



(a).



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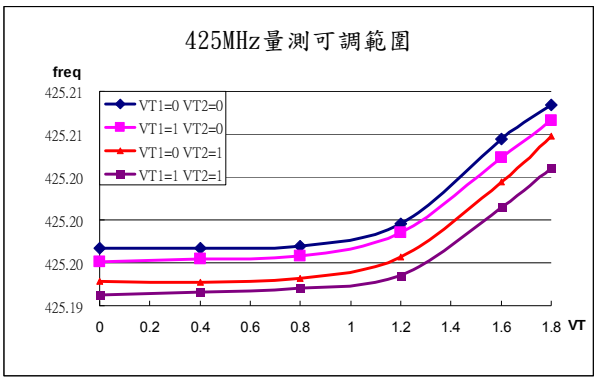

(c)

Fig. 6 (a) Measured waveform, (b) phase noise of the cross coupled SAW oscillator, (c) tuning range.

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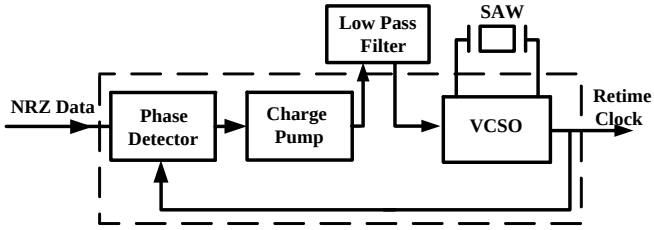

Fig. 1 Application of VCSO in giga-bit CDR

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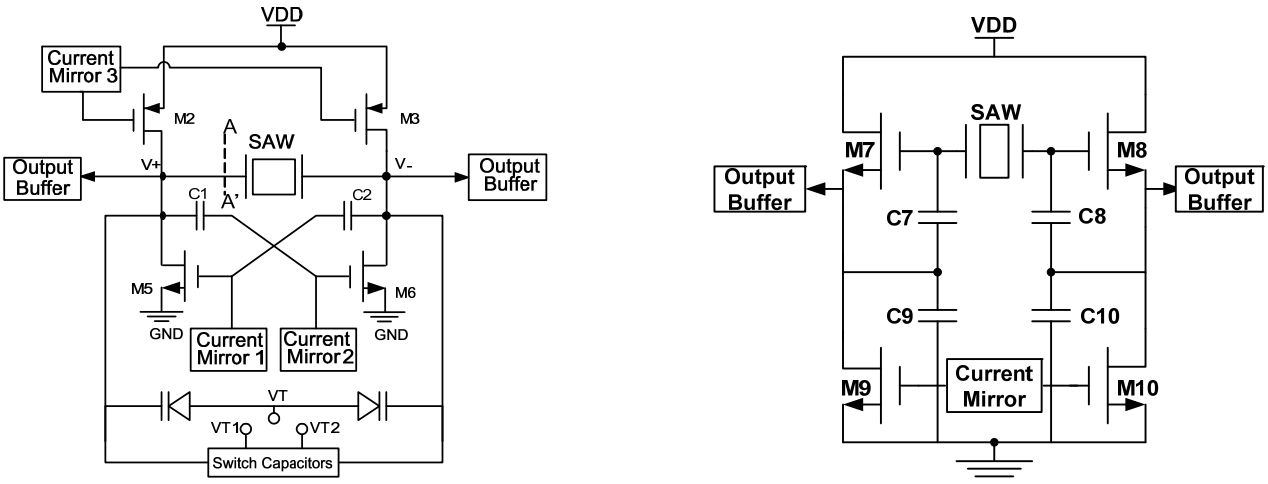

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Table I Parameters of 425MHz SAW Resonator

Co	Rs	Ls	Cs
3.8pF	10.53Ω	46.3uH	3.03fF

For clearance, the capability of the balanced Colpitts oscillator as shown in Fig. 2b is also examined. It is basically built from two single-ended Colpitts oscillator sharing one SAW resonator. M7 and M8 are the main amplifiers and M9 and M10 are the current sources. For comparison, a single ended Colpitts with similar model is firstly constructed. One pin of the resonator is connected to ground. With this success, the balanced one is easily obtained just by copying the single ended one and connecting the resonator to the gates of the main amplifiers. The SAW resonator now is re-modeled as two series resonators with center point virtually grounded [7, 8]. The ac swing across the SAW resonator in each oscillator is set equal to 100mV by trimming the aspect ratio of the transistors. The current consumptions of the core circuit without buffer are listed in Table II. Die size and phase noise are also indicated. It reveals that output power and turn-on transition in cross-coupled oscillator are the best. The turn-on transitions in cross-coupled pair and single-ended Colpitts are shown in Fig. 4. The former is about 150us in Fig. 4a and the latter is about 500us in Fig. 4b. The Balanced Colpitts is the worst. Because no strong force exists to identify the polarity, the transition period may take a long time. According to our observation, it takes about 5ms (not shown here). The cross coupled one as expected has the shorted transition time.

Phase noise is medium. The single-ended one has the best about -159.2dBc at 1Mhz offset. It seems to be due to just only one active transistor. As for the high power consumption in balanced Colpitts is due to the doubling in equivalent Co capacitance, which degrades the negative resistance.

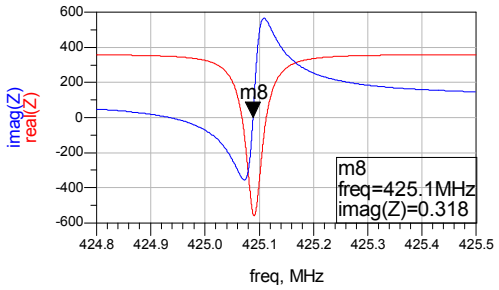


Fig. 3 The calculated negative resistance and reactance

To compare the performances, figure of merit is often used as

Table II Predicted Performances

	Cross-couple	SE Colpitts	Balanced Colpitts
CMOS Process	0.18um	0.18um	0.18um
Power Supply (V)	1.6	1.6	1.6
Current (mA) (no Buf)	3.05	1.27	5.22
Power Dissipation (mW) (no Buf)	4.88	2.032	8.352
Oscillator Frequency (MHz)	622	622	622
Phase Noise (dBC/Hz@1MHz)	-156.6	-159.282	-154.309
Output Power (dBm)	2.94	-9.725	-9.942
Transition (usec)	150	500	5000
FOM	205.6	212	200.9

$$FOM\,(dB) = 10\log\left[\left(\frac{\omega_o}{\Delta\omega}\right)^2 \frac{1}{L(\Delta\omega)\times P}\right]$$

where P is the power consumption of the core circuit, $\Delta\omega$ is the offset angular frequency from the carrier, ω_o is the center frequency, and L(Δω) is the phase noise. It reveals the cross coupled one is better than balanced Colpitts.

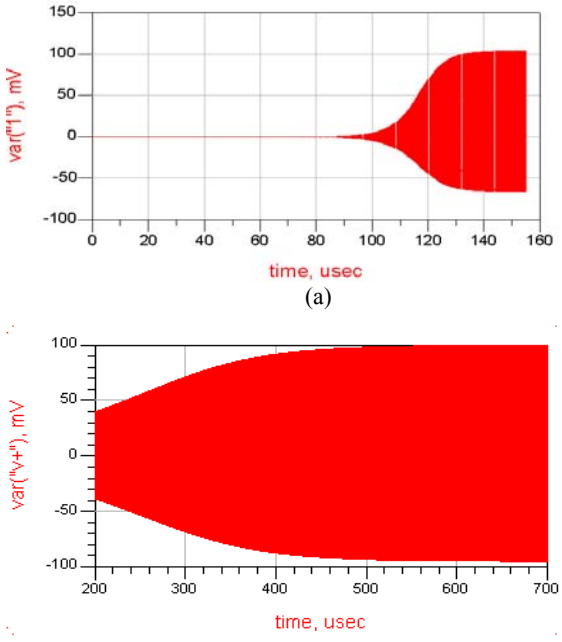


Fig. 4 Transition period in (a) cross-coupled pair and (b) single ended Colpitts oscillators.

III. Performances

The layout is illustrated in Fig. 5 with die area about 0.545×0.510mm^2. The chip is fabricated by TSMC. The measured results are shown in Fig. 6. The differential waveform with p-p 250mV is demonstrated in Fig. 6(a). The low phase noise with high quality factor SAW resonator is demonstrated in Fig. 6(b). The slope near the carrier appears 1/f^3 with noise floor around -160dBc. The continuous tuning range as shown in Fig. 6(c) is around 30ppm, depending on the size of MOS varactor, which is varied from 1.8pF to 2.45pF with VT from 0 to 1.8V. Two tuning switches are also added to increase the application. Capacitances in VT1 and VT2 switches are 0.1pF and 0.3pF, respectively.

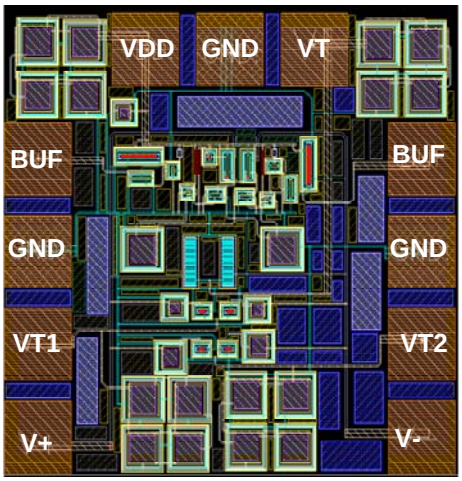


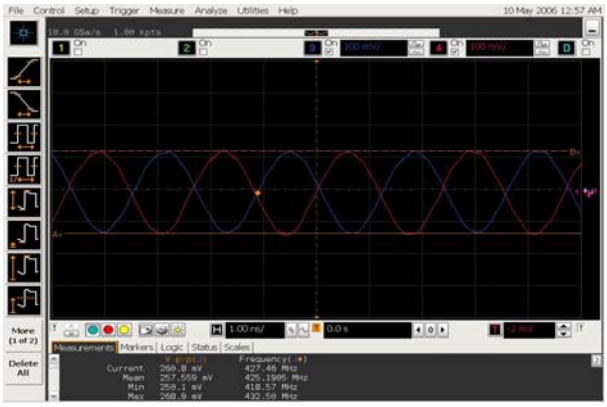
Fig. 5 Layout of the cross coupled SAW oscillator

VI. Conclusion

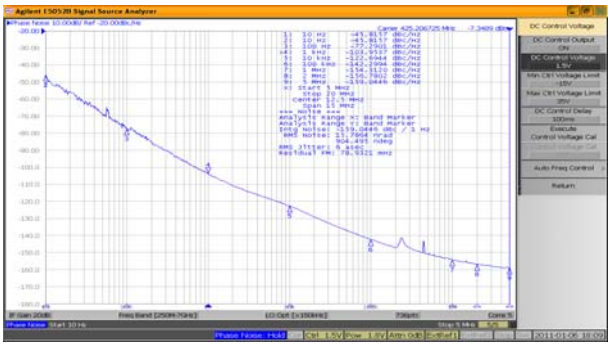
In this study a balanced VCSO using the compact cross coupled configuration is first presented. The latched problem is solved by separating carefully the drain and gate voltages. The SAW resonator acts as a parallel tank circuit to select the desired frequency. The nature of inverse polarity between gate and drain drives quickly the oscillator into steady state as compared to the balanced Colpitts one. The tuning range in this version needs to be improved in the future. Our results can be extended to other high frequency and high Q resonators such as MEMS and FBAR.

ACKNOWLEDGEMENT

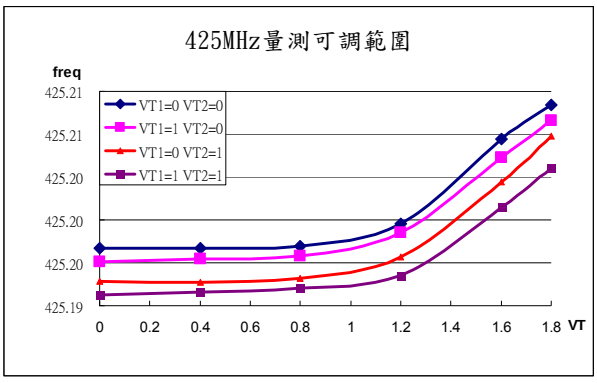
The authors would like to thank National Chip Implementation Center and National Science Council, Taiwan, R.O.C., for chip implementation and financial support.



(a).



(b)



(c)

Fig. 6 (a) Measured waveform, (b) phase noise of the cross coupled SAW oscillator, (c) tuning range.

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行政院國家科學委員會補助國內專家學者出席國際學術會議報告

100 年 07 月 11 日

報告人姓名	高曜煌	服務機構及職稱	中華大學 通訊系 教授
會議時間地點	2011/06/26-2011/06/29 Bordeaux, France	本會核定補助文號	NSC 99-2221-E-216-018
會議名稱	（中文）第九屆國際電子電機工程學會 NEWCAS 會議 （英文）9th IEEE International NEWCAS Conference,		
發表論文題目	（中文）利用 CMOS 交叉耦合對的平衡式表面聲波振盪器 （英文）Balanced SAW Oscillators with Cross-Coupled CMOS Pair		

報告內容應包括下列各項：

一、 參加會議經過

本次會議地點在法國波爾多，由於時間在暑假機位難買，最後選由新加坡航空由米蘭進巴黎出，由巴黎至波爾多則藉由法國高速鐵路 GTV 單趟約三小時。

大會由波爾多大學主辦，國際 IEEE 電路與系統學會協辦，另外有歐洲著名電子廠商贊助如 Rodhe/Schwarz、 Springer、 Thales、 RESMIQ 等，於 6/26 開始，先由四個 Tutorial 開始分別在四個重要領域討論，有

1. RF Circuit and System design in advanced Si Technologies
   題目:On-Chip RF passive Components Replacement by Their Active Counterparts: A New Trend in RFIC Design
2. RF Circuit and System design in advanced Si Technologies
   題目:Radars on Silicon]
3. Future of Wireless Communication
   題目:Cognitive and Opportunistic Radio
4. Biomedical Communication
   題目:Ultralow-Power MEMS-based Radio for WBAN

非常先進，但因需另外註冊本人未參加，接著晚上有歡迎酒會並參觀波爾多著名酒莊，感受在地文化氣息，註冊入口招牌如下圖一所示。

圖一註冊入口招牌

6/27 星期一正式開始研討會，先由 Keynote 1 開始由瑞士 CSEM 的 C. Piguet 教授講

Green Electronics

而後分兩個演講廳分別進行，分三時段共約三十篇論文，另有從下午二點至五點亦有海報討論，之後五到六點有大會主講，題目為

What kind of technology (Silicon or III-V) for the circuits and systems in the future communication satellites?

6/28 星期二一樣有兩廳三時段及海報討論外上下午各有一 Keynote，分別為 Keynote 2 為美國約翰霍浦金斯大學的 N. V. Thakor 教授講

Implanting the Brain Machine Interface: Circuits, Signals, and Systems

Keynote 3 為 THALES 公司太空部門的 Jean-Louis Roch 博士講

Sensors for Unmanned Aircraft Systems

討論結束後舉行晚宴歡迎全世界參加的學者，本次投稿 294 篇接受 130 篇接受率 44.2%。

第三天仍起始於 Keynote4 由德州理工大學的 Donald Y. C. Lee 教授主請

Design od Highly-Efficient Si-Based Transmitter ICs for Mobile Broadband Wireless Communications and Sensors Applications

之後，繼續兩廳三時段的討論，我的時段被安排在下午兩點半至兩點五十分，演講題目如圖二所示，同組有大陸東南大學李智群集成電路學院副院長，事後大家交換名片。

圖二 演講題目

基本上本學術會議大多是歐美人士，亞洲人較少，甚至沒幾個日本人，台灣方面有中央大學鄭國興教授、交通大學洪崇智教授、及台師大郭建宏等，建議可多投此會議使歐洲人更瞭解台灣。

二、 與會心得

1. 由於台灣電子科技的發展，歐美人士均有很深印象，尤其是新竹科學園區的台積電，因此每當我提及中華大學在新竹時他們均能瞭解拉近不少距離，也認為我們的資源很豐富。
2. 法國人講究生活品味及創意有自己的主見與自信。
3. 法國人的人行道相當寬，車道反而較窄，停車很不方便，但也顯示法國人以人為本的精神。
4. 法國是全世界第一觀光大國，看到來自全世界的觀光客參觀羅浮宮、凡爾塞宮、巴黎鐵塔、及時尚，真值得我們借鏡與學習

圖三 波爾多輕軌捷運非常方面

三、 回資料名稱及內容

最後，感謝國科會及學校的輔助才得以成行，討論此先進科技，攜回大會光碟一片，有興趣同仁歡迎借閱。我的電話為 5186036，Email:yhkao@chu.edu.tw 。

國科會補助計畫衍生研發成果推廣資料表

日期:2011/10/01

國科會補助計畫	計畫名稱: 具溫度補償微機電時鐘脈沖產生器
	計畫主持人: 高曜煌
	計畫編號: 99-2221-E-216-018- 學門領域: 電磁

無研發成果推廣資料

99 年度專題研究計畫研究成果彙整表

計畫主持人：高曜煌	計畫編號：99-2221-E-216-018-
計畫名稱：具溫度補償微機電時鐘脈沖產生器	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	5	5	80%		研究高Q值高穩定度的信號源,包含LC osc, SAW OSC, Crystal OSC, 及MEMS OSC, 對國內通信用高穩定度信號源可提供各種設計咨詢.
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	無

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

□達成目標

■未達成目標（請說明，以 100 字為限）

■實驗失敗

□因故實驗中斷

□其他原因

說明：

整個計畫包含二大部分,一是 MEMS 部分,另一是振盪器的推動電路. 在後半部採用 TSMC CMOS .18 製程,製作一差動式推動電路,已獲成功,並將之用以推動 SAW 共振器(400MHz),效果良好其差動的觀念可以申請專利.

至於微機電共振器部分,受 TSMC 製程的限制,在本人的環境條件下只能採用乾式蝕刻,TSMC 製程規定其間隙至少要 4um 以上,遠超過我的需求,間隙太大會使所需起動電壓過大,而且共振器等效串聯電阻太大無法起振,導到未達成目標.

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：(以 100 字為限)

本計畫中的 IC 設計部分是要克服共振器絕緣特性,並採用交叉耦合方式達到低功耗並且直接輸出的优點,雖沒用在 MEMS Resonator 上但先用在 SAW Resonator 上, 亦很有實用價值,此論文已發表在歐洲 IEEE Circuit and System 2011 會議中(2100NEWCAS),深獲同行注意並有深刻的討論.

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）(以 500 字為限)

本計畫雖沒有直接用在 MEMS Resonator 上, 但先用在 SAW Resonator 上, 亦很有實用價值,因為在高速數位通訊中均需要平衡差動輸出,如目前常見的 LVDS 信號,而目前在用高 Q 值的 Resonator 如 SAW 及 Quartz 均採用單端振盪,再轉為雙端,如此較耗費電路的面積與功率,因此本計畫中的差動電路設計部分是技術創新,是有實際應用價值.