

Reconfigurable Architecture for VLSI 9/7-5/3 Wavelet Filter

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Abstract

In this paper, the high-efficient and reconfigurable lined-based architectures for the 9/7-5/3 discrete wavelet transform (DWT) based on lifting scheme are proposed. The proposed parallel and pipelined architectures consist of a horizontal filter (HF) and a vertical filter (VF). The critical paths of the proposed architectures are reduced. Filter coefficients of the biorthogonal 9/7-5/3 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware. In the proposed architectures, all multiplications are performed using less shifts and additions. The proposed reconfigurable architecture is 100% hardware utilization and ultra low-power. The proposed reconfigurable architectures have regular structure, simple control flow, high throughput and high scalability. Thus, they are very suitable for new-generation image compression systems, such as JPEG-2000.

Keyword : Reconfigurable architecture, 9/7-5/3 discrete wavelet transform (DWT), horizontal filter (HF),