行政院國家科學委員會專題研究計畫 成果報告

整合式生產策略規劃與管控模式-從晶圓製造到覆晶封裝(I)
研究成果報告(精簡版)

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行政院國家科學委員會補助專題研究計畫 ■ 成 果 報 告
□期中進度報告

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本研究針對半導體前段晶圓製程與後段覆晶封裝製程之整合式動態的現場管控法則，包含前段投料控制以及前端現場管控模式兩個階段，透過後段瓶頸機台服務率的制定，一方面確保後段機台設備之生產產能不會損失，另一方面也考量整體系統之負荷情況，經由動態調整前段製程之在製品之加工優先，進而提供管理者在短期不更動產能水準（i.e. 不增設產能、不增加外包比例）之前提下，得以動態的舒緩或增加後段封裝製程之工作負荷，進而有效力運用公司產能進而提升工廠競爭力。

本研究之主要成果分述如下：

1. 連結晶圓製造廠前段與後段製程之管理與規劃，提供一個有系統之解決邏輯的投料法則與現場管控模式。
2. 發展瓶頸機台加工節奏之估算模式，以制訂後段製程之投料節奏，最後再加入所有產品型態影響之後，完成前段製程之投料決策模式。
3. 從TOC當中緩衝管理的角度思考，針對後段晶圓製造覆晶封裝製程生產步調，提出一套有效且合理之前段製程動態調整在製品之加工優先現場管控模式。
4. 利用eM-Plant 7.0呈現與建構前後段晶圓製造之製程過程與特性，以提供後續相關之研究平台。

中文摘要

本研究主要是針對晶圓製造與覆晶封裝之製程提出一套整合性之現場管控模式。由於晶圓覆晶製程對於高階封裝良率影響甚大，晶圓代工大廠會選擇將某些特定產品的晶圓覆晶製程自行處理，以控制產品良率。通常晶圓廠投資在各類封裝製程上的產能大小並不會如同前段的產能一般。因此，此製程常會變成產能瓶頸所在。而此一現象對於晶圓代工廠而言是一嚴重的問題，不僅拉長了產品的生產週期時間，同時也大大的降低了客戶的滿意度及其本身的競爭力。

本計畫針對在不更動產能水準的前提之下，提出一套整合式動態的現場管控法則。由具有產能缺口的後段晶圓覆晶製程作為整體生產系統現場管控的原則，並依據該製程之在製品水準動態調整前段製程在製品之加工優先順序並以DBR 排程來適時改變其投料比率與節奏，以舒緩或增加後段封裝製程之工作負荷。在此現場管控系統中，除了顧及前端晶圓製造的生產績效外，也希望後段bumping 製程通暢，以降低產品整體的週期時間及達到更多的實質產出。

關鍵詞：覆晶封裝，現場管控

Abstract

Semiconductor manufacturing is a capital and technology intensive high-tech industry with complex processes. As the technology evolution, to satisfy the high pin-count and performance requirements in the 1997 Roadmap, flip-chip became the predominant technology for chip-to-next level interconnect. Due to yield concerns, the tops foundries, such as TSMC & UMC, build their own package factories for flip-chip processes. However, the capacity of flip-chip factory is usually less than fabs' and becomes the bottleneck of all processes. It results in a large number of WIP, long cycle time and overdue orders and comes into being the disaster of foundry.

In this work, an integrated shop floor control model for wafer fabrication and flip-chip factory was developed. It included job release policy and lot priority adjustment rule of wafer fab. Due to the variability of package technique and demand, a shop floor control model will be developed to solve current production planning and control issues. A dynamic lot priority adjustment rule will be established to apply to fab. This rule will be based on the WIP level of flip chip to dynamically adjust the lot priority in wafer fabrication stage. Therefore, the buffer management is applied to control WIPs. Furthermore, DBR scheduling is used for the wafer release plan. Based on these two controls, the flow will be more smooth and efficient.

Key words: Flip-chip package, Shop floor control, Buffer management

報告內容

一、 前言

近年來全球消費性電子產業無不以輕、薄、短、小為產品的主要發展目標，因而造就了IC製造技術的蓬勃發展。根據研究指出，IC 製造技術的生命週期，通常不會超過三年(Chou et al. 2007)。因此，為維持企業競爭優勢，半導體產業內的廠商無不以導入各項先進技術作為手段。然而，在先進技術導入的中期，新世代的製程技術常常會成為整體產能的瓶頸，在產能出現缺口的同時，先進設備更替速度與需求變化之兩難問題也隨即出現。一般而言，IC 產業可分為：IC 設計、晶圓製造、IC 封裝以及最終測試四大區塊。近年來，IC 封裝產業在技術上更是發生快速的進步。觀察IC封裝技術的演進，幾乎每十年就會出現主流技術的更替。1980 年代，隨著資訊應用產業的崛起，主流封裝技術也由原本的引腳插入技術(Pin Through Hole, PTH)演進成為表面黏接技術(Surface Mount Technology, SMT)；1990 年代，隨著IC 體積逐漸縮小，SMT技術也逐漸被球閘陣列封裝技術(Ball Grid Array, BGA)所取代(張錦煌，2006)。在進入21 世紀之後，傳統打線技術(Wire Bounding)以無法負荷越來越高的接腳數目以及效能，因此，可以預期打線技術將被覆晶封裝(Flip Chip)技術所取代。覆晶封裝技術的關鍵在於晶圓凸塊製程(Wafer Bumping)，其概念是將由錫鉛構成的凸塊(Bump)或錫球排列於晶圓表面後，再植入晶片的焊墊(Bonding Pad)上方，以便封裝時可利用熱能將凸塊熔融，促使元件與基板結合。在先進製程尚未充足設置以及高階封裝產品需求增加的交互影響之下，幾乎各封裝廠wafer bumping 製程的產能利用率都居高不下，根據資料，2004上半年各廠在此製程之產能利用率幾乎都在95%以上(楊雅嵐，2004)，除此之外如圖1(王旭昇，2007)所示業界對於wafer bumping 從2005 至2010 之市場規模預估趨勢，其產值與年成長率的表現上也顯示出其研究之價值。

資料來源：IEK(05/2007)，IBT Research整理

圖1. 2005~2010 年封裝市場規模預估

然而由於 wafer bumping 製程對於高階封裝良率影響甚大，晶圓代工大廠通常會選擇將某些特定產品的bumping 製程自行處理，而不交由下游封裝廠進行代工，以控制其產品

良率。在此生產策略之下，晶圓代工廠內所生產之產品可粗略劃分為：不需經過bumping製程、需經過bumping 製程但可外包給下游封裝廠以及需經過bumping 製程且必須自行完成等三類產品。然而，一般而言，晶圓製造廠投資在各類封裝製程上的產能大小並不會如同前段(晶圓製造)的產能一般。對於必須自行完成bumping製程的產品而言，此製程常常會變成產能瓶頸所在，不但增加生產時間，在缺乏完善的生產規劃之下，也造成過多的在製品堆積。此外，對於晶圓製造廠而言，晶圓製造部分往往被當作是重點所在，所以大部分的資源與努力都集中於此。而覆晶封裝部分卻只能承接晶圓製造完成的成果，所以在產能不足的情形下，生產績效就更加的雪上加霜了。然而，對整個企業而言，產品若不能順利及時地從覆晶封裝加工完成仍無法出貨。在不經過產能擴充或外包的前提之下，要解決上述晶圓廠中 wafer bumping 產能不足的問題，最有效的方法為透過產品組合規劃與現場派工的動態調整。在過高的設備資本投資的影響下，晶圓廠會要求各工作站盡可能提高其機台使用率(Wu et al., 2005)。然而，此舉卻會增加產能已遠小於前段製程的後段封裝程序之生產負荷，致使產能缺口的問題更加嚴重。再者，在晶圓廠現行的現場管控法則中，也大多以降低生產時間或增加產出等目標作為規劃原則，並且大多以前段製程作為規劃標的，鮮少顧及產能不足的後段封裝製程，致使大部分產品雖能快速完成前段晶圓製造製程，卻堆積在後段封裝製程中。但過去之研究往往針對某段的環境進行探討，對於將其上游之環境合併加以考量之研究則較為不足。然而晶圓製程到覆晶封裝實為一連續的製造流程，若產品組合規劃與外包策略的目標只為了讓前段製程(晶圓製程)生產績效維持在一定的水準，則對於後段製程而言必產生不良的影響。再加上半導體產業的市場環境因素多變，其不良的決策勢必更加嚴重地影響到企業未來的經營。過去亦有許多研究試圖以現場管控的手法解決晶圓製造的複雜環境中生產績效提升之問題。Hung and Chang (2002)提出一套修正的最小寬鬆時間法則與最小剩餘加工時間法則，期望能達到縮短生產時間的目標；Bowman (2002)則是以JIT 為基礎，提出一套投料控制法則，避免瓶頸機台閒置以達成最大產出；Louw and Page (2004)則是利用等候網路模型，計算半導體晶圓廠在以TOC為基礎之管控法則下，緩衝時間大小之制訂法則。然而，這些相關研究卻未針對橫跨二生產區段之生產環境(e.g. 晶圓製造連接封裝製程)做進一步討論。再者，也未就產能不足情況下，現場管控該如何調整做更深入的探討。Chou 等學者(2007)曾經說明，如同半導體這類產能設置週期時間繁長、資本投資龐大的產業，若將各類管理活動分開獨立進行規劃，將無法獲得一個有效的解決方法。

二、 研究目的

綜觀上述問題背景，本研究之主要目的在於在不更動產能水準（i.e. 不增設產能、不增加外包比例）之前提下，提出一套整合式動態的現場管控法則。由具有產能缺口的後段bumping 製程作為整體生產系統現場管控的原則，並依據該製程之在製品水準動態調整前段製程在製品之加工優先順序並改變先前定義之三類產品之投料比率與節奏，以舒緩或增加後段封裝製程之工作負荷。在此現場管控系統中，除了顧及前端晶圓製造的生產績效外，也希望後段bumping 製程通暢，以降低產品整體的週期時間及達到更多的實質產出。本研究以半導體製造廠中從晶圓製造到 wafer bumping 製程為例，在需求高度

不確定、生產技術快速更替的環境下之產能缺口問題中，提出一套系統化解決模式。吾人期望此解決模式不但能應用於半導體產業，亦可適用於具有相同產業特色之其他產業當中。

三、 研究方法

本研究之主要目的為：在高度需求不確定以及高投資風險的環境下，針對高階覆晶封裝製程產能不足之晶圓製造廠，發展一套現場管控模式。一般而言，半導體廠中之前段晶圓製造製程（後文中簡稱為『前段製程』）在產能設置上，將會遠大於後段晶圓封裝製程（後文中簡稱為『後段製程』），特別是在先進封裝技術上，前、後段的產能差距更是明顯。吾人在研究中曾說明，在這樣的生產環境下，系統內將存在著三類產品，而在這些不同的產品類型中，『必須經過 bumping 製程且無法外包』之產品，由於先進封裝製程產能不足使然，其生產瓶頸必然出現在後段製程中。吾人針對此問題實際訪查晶圓代工廠發現，由於生產系統中只存在部分產品必須採用高階封裝，再加上管理者一般都認為半導體製造的關鍵因素存在於前段製程當中，因此，晶圓廠的生產規劃工作一般還是以前段製程作為主要規劃準則。此舉無疑更加深後段製程產能不足的影響，因而造成後段製程在製品累積數量過多、必須自行處理先進封裝製程的產品生產時間過長的問題。

對於必須完整通過前、後段製程之產品而言，後段高階製程必然為影響生產績效最顯著之因子。經過分析、整理後吾人發現，目前在此問題上的管理難題來自於以下關鍵因素：

1. 前段製程之投料未考量後段製程產能大小

從限制理論(Theory of Constraint, TOC)的觀念中，吾人得知系統之績效表現取決於系統之制約因素(constraints, i.e. 生產系統中之瓶頸機台)，並且其他非制約因素必須全力配合制約因素(Goldratt, 1986)。一般來說，後段覆晶封裝製程之瓶頸加工站為 Sputter(金屬濺鍍)加工站，在此加工站產能已然不足的情形下，後段製程之投料速率更加必須依據 sputter 工作站控制投料速率(Wu and Yeh, 2006)。然而，後段製程之投料來自於前段製程之產出，因此，若前段製程在投料控制上沒有進一步考慮後段製程產能限制，任何生產規劃活動將無法有效進行。

2. 前段製程之現場派工未考量後段之現場狀況

在後段製程中為保護系統瓶頸，在 sputter 機台前會存在著一定數量在製品，以確保該機台不閒置。然而，若在製品數量過多，卻反而會造成產品之等候時間過長，造成生產週期時間增加。雖然從等候理論(Queuing Theory)的基本定義中，一個系統的產出率將等同於原始投料速率(Connors et al., 1996)。然而，由於晶圓製造前段製程環境極其複雜並充滿許多影響生產週期時間之因素(Russ and John, 2003)，致使產品產出間隔時間將會具有相當程度之變異性。因此，即使在投料數量已然超過後段生產系統負荷的情況下，後段製程中的在製品數量仍然會具有相當程度的波動。在這樣的影響之下，前段製程若缺乏以後段製程之在製品數量動態調整必須經過後段製程之產品的派工邏輯，則將無法保護後段瓶頸機台，甚至影響其他種類產品之生產週

期時間的後果。

3. 不良的產品組合與後段產能不足

從過去產業歷史資料發現，高階覆晶封裝產品所占的產品比重有逐年升高的趨勢，近三年之需求成長率約在 30%左右，然而，這段期間之供給成長率卻只有 20%(盧慶儒，2006)。而在這些高階覆晶封裝產品當中，有某些部分在顧客的要求或晶圓製造廠基於良率控制考量之下，其封裝製程無法由封裝廠進行代工，而必須自行完成這部分的製程。若晶圓代工廠在市場定位上不加以考量後段製程的產能限制，生產系統內之產品組合必然無法做有效的規劃。以吾人訪查的某晶圓代工廠為例，該廠商必須由自己完成覆晶封裝的產品月需求約在 4 萬片左右，然而，其後段覆晶封裝的產能卻不到 3 萬片。在如此錯誤的產品組合與產能設置之下，即使有正確的投料控制或管控法則，亦無法獲得良好的績效。

吾人認為，對於高階覆晶封裝產品在晶圓製造場所造成的管理難題，必須從前段製程中的現場管控法則與其投料控制提出一完整解決方法，方能有效解決。其本次相關研究結果已發表於The Tenth International Conference on Information and Management Science (IMS2011)，關於研究概念架構如下所示，其細部之資料請參閱附錄之文章。

1. 前段製程之投料控制

從上述問題分析結果中吾人認為，對於必須自行完成覆晶封裝之產品的投料速率必須由後段製程之瓶頸機台服務率決定。然而，瓶頸機台之服務率除受到加工時間影響之外，還必須考慮機台產能損耗，例如，機台當機影響。因此，在瓶頸機台的服務率計算上必須以機台之可用率修正之。然而，機台可用率為一統計平均值，約只佔 68%的累積機率，因此，吾人進一步採用 Tu and Li(1998)所提出之管理者信心水準修正模式進行機台可用率之修正。其概念可由下列數學式表示之：

$$\mu_{sputter} = \frac{1}{(\tau_{sputter} / A_{sputter}) \times \ln \frac{1}{1-\alpha}}$$

其中，

$\mu_{sputter}$ ： 後段製程中 Sputter 工作站之服務率

$\tau_{sputter}$ ： 後段製程中 Sputter 工作站之平均服務時間

$A_{sputter}$ ： 後段製程中 Sputter 工作站之可用率

α： 管理者信心水準

在計算得知後段製程瓶頸機台之生產節奏之後,前段製程則必須以此節奏進行投料。然而，在前段製程中除了必須自行完成覆晶封裝製程之產品之外，還包含其餘二項種類之產品。再者，前段製程之產能遠大於後段製程。因此，吾人即可將其於二類之產品填滿前段扣產能扣除已劃分給覆晶封裝產品的部份。其邏輯如下圖示：

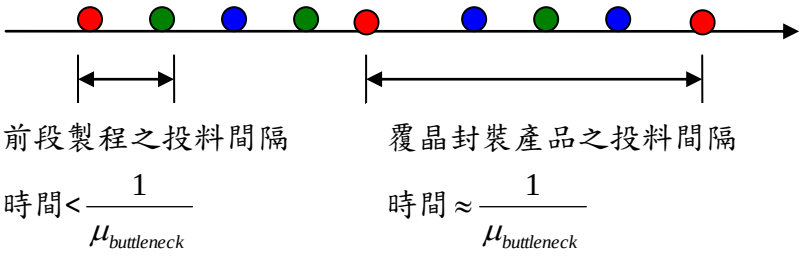

圖 2. 前段製程投料節奏示意圖

2. 前段製程之現場管控法則

前段製程除投料速率必須考量後段製程產能之外，現場管控法則亦必須考量後段製程之在製品水準進行動態調整。為了同時顧及避免瓶頸機台閒置以及產品等候時間過長的目標，吾人採用 TOC 當中的緩衝管理(buffer management)概念，進一步以在製品存量警示上界與下界將後段製程在製品水準化分成三個區域,分別為:加速區、正常區與舒緩區。當後段在製品水準落於加速區（小於警示下界）時，表示後段製程在製品存量不足以保護瓶頸機台，因此，前段製程必須提高覆晶封裝產品之加工優先順序，使其儘速完成前段製程，以增加後段製程之在製品存量。反之，若後段製程在製品水準落於舒緩區（大於警示上界）時，前段製程則必須降低覆晶封裝產品之加工優先順序,以舒緩後段製程之工作負荷。而在警示上界於下界計算邏輯上，由於造成瓶頸機台閒置最大的原因來自於上游機台的產能損耗，因此，吾人將瓶頸機台上游各加工站之期望損耗產能加總後，再減去瓶頸機台之產能損耗，即為保護瓶頸機台所需之在製品存量，亦即警示下界。而警示上界的算法，主要邏輯為：當瓶頸機台保持於某產能利用率水準時，藉由等候模型計算其平均等候線長度，此等候長度即為此產能利用水準下之合理在製品水準，若將合理在製品水準呈上一寬放因子，即為在製品警示上限。

四、 結果與討論

由於在半導體產業之中，唯有不斷的提升製程能力與提升生產之績效，方能在瞬息萬變的市場中佔有一席之地，然而製程能力的提升非短期間內即可完成，因此在某些短期的生產管控應變方面，勢必需要一套合理的運作邏輯，本研究針對半導體前段晶圓製程與後段覆晶封裝製程之整合式動態的現場管控法則，包含前段投料控制以及前端現場管控模式兩個階段，透過後段瓶頸機台服務率的制定，一方面確保後段機台設備之生產

產能不會損失，另一方面也考量整體系統之負荷情況，經由動態調整前段製程之在製品之加工優先，進而提供管理者在短期不更動產能水準（i.e. 不增設產能、不增加外包比例）之前提下，得以動態的舒緩或增加後段封裝製程之工作負荷，進而有效力運用公司產能進而提升工廠競爭力。

由於製程世代的轉換對於半導體產業的永續存在著一定程度影響，如何適時安排新製程的導入，使得在轉換時公司依舊保持著一定的競爭優勢，快速的反應需求的變動，將生產能力調整到最適宜的，不至於因新製程的導入而引發更多的問題，實為未來研究值得探討之方向。

就本質而論，本計畫之研究成果同時具有實務及學術價值。在實務方面，本計畫之成果提供晶圓廠對於覆晶封裝之產能現場管控方式能有所憑藉；在學術上，本研究提供一套以緩衝管理理論為基礎，應用於半導體廠中之前後段晶圓製造製程現場管控之概念。此外，本研究亦已將研究成果發表於國際學術研討會之中。

本研究之主要成果分述如下：

1. 連結晶圓製造廠前段與後段製程之管理與規劃，提供一個有系統之解決邏輯的投料法則與現場管控模式。
2. 發展瓶頸機台加工節奏之估算模式，以制訂後段製程之投料節奏，最後再加入所有產品型態影響之後，完成前段製程之投料決策模式。
3. 從TOC當中緩衝管理的角度思考，針對後段晶圓製造覆晶封裝製程生產步調，提出一套有效且合理之前段製程動態調整在製品之加工優先現場管控模式。
4. 利用eM-Plant 7.0呈現與建構前後段晶圓製造之製程過程與特性，以提供後續相關之研究平台。

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附　錄

附 件 一

Shop Floor Control Model for Wafer Fabrication and Flip Chip

Shop Floor Control Model for Wafer Fabrication and Flip Chip

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Abstract: Semiconductor manufacturing is a capital and technology intensive high-tech industry with complex processes. As the technology evolution, to satisfy the high pin-count and performance requirements, flip-chip became the predominant technology for chip-to-next level interconnect. Due to yield concern, the tops foundries, such as TSMC & UMC, build their own package factories for flip-chip processes. However, the capacity of flip-chip factory is usually less than fabs' and becomes the bottleneck of all processes. It results in a large number of WIP, long cycle time and overdue orders and comes into being the disaster of foundry.
In this study, a shop floor control model for wafer fabrication and flip-chip factory will be developed. It includes job release policy and lot priority adjustment rule of wafer fab. Due to the variability of package technique and demand, a shop floor control model will be developed to solve current production planning and control issues. A dynamic lot priority adjustment rule will be established to apply to fab. This rule will be based on the WIP level of flip chip to dynamically adjust the lot priority in wafer fabrication stage. Therefore, the dynamic buffer management will be applied to control WIPs of fab. In this work, the lower bound and upper bound of WIP in front of constraint machine will be set and to divide the WIP level into three zones, red, yellow and green zone. When WIP level falls into red zone (less than lower bound), lot priority in wafer fabrication stage should be set higher. On the contrary, if WIP level falls into green zone (more than upper bound), lot priority can be set lower. Furthermore, DBR scheduling concept will be applied to the wafer release plan for flip-chip factory. According to the pace of the constraint machine to release wafer, it can make sure to maximize the factory throughput and to keep the WIP lower. Hence, based on these two controls, the flow will be more smooth and efficient both on wafer fabrication and flip-chip factory.

Keywords: Wafer fabrication, Flip-chip package, Shop floor control, Dynamic buffer management, DBR scheduling

I. Introduction

Recently, the market needs to drive consumer electronic products to be smaller, faster and higher functionality. The trend in microelectronic packaging technology is toward miniaturization and high performance. In order to keep the competition, IC companies are forced to introduce advance technology no matter in wafer fabrication, probe, testing or assembly. However, the new generation technology always becomes the bottleneck of the whole process when an advanced technology is first introduced. Due to the uncertainty of future demand, to speed the technology migration rate or just keep in watch will be a dilemma when the capacity of new technology shortage happens. This phenomenon is also occurred in the flip chip process. As the technology evolution, to satisfy the high pin-count and performance requirements, flip-chip became the predominant technology for chip-to-next level interconnect. Flip chip bonding was first introduced by IBM in 1964. It was called controlled collapse chip connection (C4) by IBM, in which the flow of the solder bump during soldering is controlled by the die solder bump volume, area of the solder wet-table pad on the substrate, the die weight and the solder surface tension[14]. Due to yield concern, the tops foundries, such as TSMC & UMC, build their own package factories for flip-chip processes. Under this production strategy, the products in foundry can be separated into two parts, non-bumping process and bumping process. Nonetheless, the capacity of flip-chip factory is usually less than fabs' and becomes the bottleneck of all stages. It results in a large number of WIP, long cycle time and overdue orders and comes into being the disaster of foundry. The most effective solution for the issue is to increase the capacity of flip chip factory. As well known, the capacity plan is a long term plan. It means the capacity can not be increased within a short time. Especially, when the market demand is instinct with uncertainty, it is hard to decide to increase capacity. Under this situation, a suitable shop floor control model for wafer fabrication and flip-chip factory will be the best way to relieve the disaster of foundry.
In the past studies, all shop floor control models are designed for only one kind of factory, especially for fab [1], [8], [11]. As we know, wafer fabrication is a capital intensive industry. Therefore, to fully utilize the production resources to get the maximum output and shortening cycle time are the major targets of all fabs [4], [5], [10]. Nevertheless, although the fabs perform well, the bumping products are still pilled in the flip chip factory. From the

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company management point of view, this kind of orders will take a long cycle times or even be overdue. Hence, a shop floor control model links with wafer fabrication and flip chip factory is needed. It should manage not only fab production but also flip chip portion.

Accordingly, an integrated shop floor control model is developed in this work. It includes job release policy and dynamic lot priority adjustment rules. Both release policy and priority rules are based on the bottleneck machine (platting equipment) to set the production smoothness f the whole processes. Under this control, both fab and flip chip factory can get the better performances. This paper was structured as follows. In the next section, the job release policy and dynamic lot priority adjustment rules are proposed. In section 3, a numerical example is presented to demonstrate this control model. Finally, the summary and future researches are included in Section 4.

II. Integrated Shop Floor Control Model (isfc)

Generally, wafer fabrication and flip chip factory are two separated factories and managed by different teams and rules. However, the flip chip factory should take the result of fab. If the production management of fab focuses on their own factory only, the chip flip factory will suffer the variability of fab's output. Therefore, an integrated shop floor control model to link with fab and flip chip factory is very important for the whole performance. In this model, there are two parts of rules, including job release policy and lot priority adjustment rule of wafer fab. Although these rules all will be acted in fab, the indicator will be the bottleneck of whole processes. In other word, it will be the plating equipment in this model. The details are described as follows.

A. NOTATION

The following terminology is required for the capacity support control model.

$\lambda_{bumping}$: Arrival rate of bumping products in fab

$\mu_{bottleneck}$: Service rate of plating workstation in flip chip factory

$\tau_{bottleneck}$: Service time of plating workstation in flip chip factory

$A_{bottleneck}$: Availability of plating workstation in flip chip factory

M : Number of bottleneck machines

s : Lower bound of WIP level

ECL_i : Expected capacity loss of feeder machines of bottleneck machine

$ECL_{bottleneck}$: Expected capacity loss of bottleneck machine

PT_j : Processing time of upstream machine

$PT_{bottleneck}$: Processing time of bottleneck machine

$MTTR_i$: Mean time to repair(MTTR) of Feeder machines

S : Upper bound of WIP level

EQ : Expected queue length of bottleneck machine

$\rho_{bottleneck}$: The utilization goal of bottleneck machine

ω : allowance

B. RELEASE POLICY

Based on TOC (Theory of Constraints) concept, it reveals that the system performance is decided by system constraint (i.e. the bottleneck of the production system) and all non-constrains should subordinate the constraint [6], [7]. Generally, the bottleneck of flip chip factory is the plating workstations. Hence, the wafer release tempo should be based on the production rate of plating workstation [9], [13]. However, as mentioned above, the release of flip chip factory comes from the output of fab. If the factor of flip chip factory's constraint can't be taken into account to the release policy of fab, any production planning can't be effective. Therefore, the release rate of bumping products to the fab should be based on the production rate of plating workstation. Basically, the major factor affecting the production rate is the processing time. In addition, the capacity loss, for example machines breakdown, will also impact the production rate. Hence, the production rate of bottleneck should be modified by the availability of workstation. Based on these concepts, the production rate of plating workstation can be identified as the following equation.

$$\lambda_{bumping} = \mu_{bottleneck} = \frac{M}{(\frac{\tau_{bottleneck}}{A_{bottleneck}})} \quad (1)$$

It can be made a conclusion that the bumping products have to be released by the same rate as the service rate of the bottleneck of flip chip factory. As we know, there is another kind of products processed in fab and the capacity of fab is more than flip chip factory. Therefore, the actual arrival rate in fab will larger than the arrival rate of bumping products. The relation can be described as follows.

$$\lambda_{fab} = \lambda_{bumping} + \lambda_{non-bumping} \quad (2)$$

C. DYNAMIC LOT PRIORITY ADJUSTMENT RULE

The production environment is full of uncertainty and unpredictable events, such as machine breakdown, material shortage, staffs' leaving,…etc[11]. Although the release policy is perfect, the production schedule is still disturbed by the unpredictable events. Finally, the execution results are far away from the plan. Shop floor control is the best way to amend this result. Same as the release policy, the shop floor control rules should be also taken the status of flip chip factory into account and have to adjust the production rate of bumping product dynamically in wafer fabrication stage. In order to avoiding the starvation of bottleneck machine and lengthening the waiting time of bumping products in flip chip factory, the concepts of buffer management in TOC (Theory of Constraints) are applied. The WIP level of bottleneck machine is divided into three zones by lower bound and upper bound, names red, yellow and green zone. When the WIP level is falling into the red zone, it means that the WIP level is too low to protect the bottleneck machine from starvation. Hence, the priority of bumping products should be higher to push the WIP into flip chip factory quickly. On the contrary, if the WIP level is falling into the green zone, it stands for the WIP level is too high. Too many WIPs waiting in front of bottleneck machine will increase the cycle time of products [2], [4], [5], [12]. Therefore, the priority of bumping products should be lower down in wafer fabrication stage to decrease the arrival rate of bumping products into flip chip factory.

Based the description above, the critical point of this dynamic lot priority adjustment rule is how to define the lower bound and upper bound of WIP level. The purpose of lower bound is to avoid the starvation of bottleneck machine. The major cause of machine starvation is the capacity loss of feeder machines. Under this situation, the lower bound will be the amount of WIP to cover the capacity loss of feeder machines. Besides, although the priority of bumping products are heightening in wafer fabrication stage and make them to flow into flip chip factory quickly, the bumping products still should take time to arrive the bottleneck machine. Therefore, the time from the first workstation to the bottleneck has to take into consideration. Accordingly, the lower bound of bottleneck can be described as the following equations.

$$s = (\sum_{i=1}^{n} ECL_i - ECL_{bottleneck}) + \frac{\sum_{j=1}^{m} PT_j}{PT_{bottleneck}} \quad (3)$$

$$ECL_i = MTTR_i \times \mu_i \times (1 - A_i) \quad (4)$$

The major purpose of the upper bound is to prevent the long cycle time of products. The queuing theory is applied to the formulation. Based on the queuing theory, waiting time of products is decided by the utilization of equipment. When the managers set the goal of cycle time of products, the utilization of equipment can be calculated. The expected queue length can also be derived based on the utilization of equipment. Because the expected queue length is just an average number, the allowance is put into the upper bound equation and expresses as follows.

$$S = EQ(\rho_{bottleneck}, M) \times \omega \quad (5)$$

$$EQ(\rho_{bottleneck}, M) = \frac{P \times \left(\frac{\lambda}{\mu}\right) \times \rho}{M! \times (1-\rho)^2} \quad (6)$$

$$P = ((\sum_{n=0}^{M-1} (\frac{1}{n!} \times \left[\frac{\lambda}{\mu}\right]^n)) + \frac{1}{M!} \times \left[\frac{\lambda}{\mu}\right]^{Mn} \times \frac{M \times \mu}{M \times \mu - \lambda})^{-1} \quad (7)$$

$$\rho = \frac{\lambda}{M \times \mu} \quad (8)$$

III. **Numerical Example**

Appendix 1, 2 and 3 show illustrate the preliminary data concerning the example, including information about the master production schedule (MPS), the machines and the routing of products. The measure unit of releasing batch into factory is "lot". A lot includes 25 wafers. The release policy is of uniform distribution. A wafer factory can normally be divided into seven areas, with more than one machine in each. Machines in the same area perform the same functions. The processing time is defined by recipe in wafer fabrication, however, it is defined by equipment in flip chip factory.

This example assumes that the equipment of GP10 (Plating equipment) is the bottleneck machine in flip chip factory. Therefore, the release rate of bumping products in wafer fabrication is as follows.

Based on equipment list of wafer bumping, it shows that the WPH (Wafer Per Hour) of GP10 by product are as follows.

Product	Service Time(hrs)
A	(3.316+3.125+6.812)/3=4.418
B	(6.812+4*4.587)/5=5.032
C	(6.812+4*4.587)/5=5.032
D	4.587

$$\tau_{GP10} = \frac{540}{1141} \times 4.418 + \frac{420}{1141} \times 5.032 + \frac{200}{1141} \times 5.032 + \frac{1}{1141} \times 4.587 = 4.752$$

$$A_{GP10} = (0.91 + 0.94 + 0.93 + 0.93 + 0.91 + 0.9 + 0.93 + 0.93)/8 = 0.92$$

$$\lambda_{bumping} = \mu_{GP10} = \frac{8}{(\frac{4.752}{0.92})} = 1.55(lot/hour)$$

Based on the equation 3 and 5, the lower bound and upper bound of GP10's WIP level can be derived as follows.
Assume ω=1.1
Average Process Time of equipment in flip chip factory:

Equipment	Average Process Time (Hrs)
GP1	0.246
GP2	1.041
GP3	1.520
GP4	0.650
GP5	0.840
GP6	1.220
GP7	1.294
GP8	0.703
GP9	1.420
GP10	4.752
GP11	1.826
GP12	1.021
GP13	1.125
GP14	2.013

The expected capacity loss of feeder machines :

$$\sum_{i=1}^{n} ECL_i = ECL_{GP8-1} + ECL_{GP8-2} + ECL_{GP8-3} + ECL_{GP8-4}$$
$$= 110.4*1/0.703*(1-0.9) + 151.8*1/0.703*(1-0.9) + 100.2*1/0.703*(1-0.9) + 156.6*1/0.703*(1-0.9) = 73.8$$

$$ELC_{bottleneck} = 273*1/3.316*(1-0.91) + 301.8*1/3.125*(1-0.91) + 285.6*1/6.812*(1-0.94) + 309*1/4.587*(1-0.93) + 268.2*1/4.587*(1-0.93) + 292.2*1/4.587*(1-0.93) + 300.6*1/4.587*(1-0.93) + 745.8*1/4.587*(1-0.90) = 52.73$$

The time from the first workstation to the bottleneck:

$$\sum_{j=1}^{m} PT_j = PT_{GP-1} + PT_{GP-2} + PT_{GP-1} + PT_{GP-3} + PT_{GP-4} + PT_{GP-5} + PT_{GP-6} + PT_{GP-7} + PT_{GP-8} + PT_{GP-9} + PT_{GP-8} = 9.86(Hrs)$$

Therefore, the lower bound can be defined as follows.

$$s = 73.8 - 52.73 + 9.86/4.752 = 23.15 \approx 24(lots)$$

$$P = ((\sum_{n=0}^{7} \frac{1}{n!} \times \left[\frac{1.5178}{0.1936}\right]^n) + \frac{1}{8!} \times \left[\frac{1.5178}{0.1936}\right]^8 \times \frac{8 \times 0.1936}{8 \times 0.1936 - 1.5178})^{-1} = 0.000053$$

$$\rho = \frac{1.5178}{8 \times 0.1936} = 0.98$$

$$EQ(\rho_{bottleneck}, M) = \frac{0.000053 \times \left(\frac{1.578}{0.1936}\right) \times 0.98}{8! \times (1-0.99)^2} = 45.9$$

$$S = EQ(\rho_{bottleneck}, M) \times \omega = 45.9 \times 1.1 = 50.49 \approx 51(lots)$$

IV Conclusion

In this work, an integrated shop floor control model between wafer fabrication and flip chip is established to enhance the whole production performance. There were two control rules are developed, wafer release policy and dynamic lot priority adjustment rules. Both of them are based on the bottleneck of whole production line to manage the production tempo. Through these two control rules, the production performances of wafer fabrication and flip chip factory will be improved.
Regarding to the future works, there are two points can be considered. The first one is the effect of deviation of wafer release on the production performance. Actually, the studies of release policy in most of researches focus the mean of arrival rate. However, the sources of performance variation come from the deviation of control factors. Therefore, the sensitivity of deviation of arrival rate is

worth studying. Besides, the arrival pattern is another factor which will affect on the production performance. Although the arrival pattern can not be well controlled in the real life, it can be studied how the performance is affected. Finally, this result can be used to adjust the shop floor status.

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Appendices

Appendix 1: Master Production Schedule

Wafer fabrication

Product	Demand(lot/month)
Non-bumping	2282
bumping	1093

Wafer bumping

Product	Demand(lot/month)
A	520
B	420
C	200
D	1

Appendix 2: Machine information
Wafer fabrication

Equipment	M/C Qty	MTTR (Hr)	MTBF (Hr)	Availability
ADI	19	1.5	48.50	0.97
AEI	10	1	49.00	0.98
cvd-1	14	3	72.00	0.96
cvd-clean	8	1	49.00	0.98
diff-1	55	5	95.00	0.95
diff-clean	15	1	49.00	0.98
dry-1	46	2.5	25.28	0.91
imp-1	6	2	20.22	0.91
imp-2	4	1.5	48.50	0.97
photo	49	2	38.00	0.95
pvd-1	4	1	49.00	0.98
pvd-clean	3	0.5	49.50	0.99
wet-1	25	2.5	39.17	0.94

Wafer bumping

Equipment	M/C Qty	Process Time (Hrs)	MTTR(Hrs)	AVAIL(%)
GP-1-1	1	0.246	70.20	0.92
GP-1-2	1	0.246	61.80	0.92
GP-2 -1	1	1.111	249.00	0.57
GP-2 -2	1	1.045	208.20	0.59
GP-2 -3	1	0.968	211.20	0.57
GP-3 -1	1	1.644	65.40	0.82
GP-3 -2	1	1.535	66.00	0.82
GP-3 -3	1	1.382	64.80	0.82
GP-4 -1	1	0.767	56.40	0.85
GP-4 -2	1	0.533	57.00	0.85
GP-5 -1	1	0.966	82.20	0.87
GP-5 -2	1	0.714	59.40	0.90
GP-6 -1	1	1.268	55.80	0.90
GP-6 -2	1	1.268	88.80	0.90
GP-6 -3	1	1.125	166.80	0.90
GP-7-1	1	1.294	225.60	0.90
GP-7-2	1	1.294	243.00	0.90
GP-7-3	1	1.294	191.40	0.90
GP-8-1	1	0.703	110.40	0.90
GP-8-2	1	0.703	151.80	0.90
GP-8-3	1	0.703	100.20	0.90
GP-8-4	1	0.703	156.60	0.90
GP-9-1	1	1.420	0.00	0.94
GP-9-2	1	1.420	0.00	0.94
GP-9-3	1	1.420	74.40	0.94
GP-9-4	1	1.420	140.40	0.94
GP-9-5	1	1.420	56.40	0.94
GP-10 (A) -1	1	3.316	273.00	0.91
GP-10 (A) -2	1	3.125	301.80	0.91
GP-10 (A/ B/ C)	1	6.812	285.60	0.94
GP-10 (B/ C)-1	1	4.587	309.00	0.93
GP-10 (B/ C)-2	1	4.587	268.20	0.93
GP-10 (B/ C)-3	1	4.587	292.20	0.93
GP-10 (B/ C)-4	1	4.587	300.60	0.93
GP-10 (D)	1	4.587	745.80	0.90
GP-11 -1	1	1.561	75.60	0.85
GP-11 -2	1	1.561	227.40	0.85
GP-11 -3	1	1.561	127.20	0.85
GP-11 -4	1	2.621	137.40	0.85
GP-12-1	1	1.021	195.00	0.86
GP-12-2	1	1.021	151.20	0.86
GP-12-3	1	1.021	333.00	0.86
GP-13-1	1	1.125	253.20	0.61
GP-13-1	1	1.125	277.20	0.61
GP-13-1	1	1.125	253.80	0.61
GP-14-1	1	2.013	250.20	0.89
GP-14-2	1	2.013	225.00	0.89
GP-14-3	1	2.013	319.20	0.89
GP-14-4	1	2.013	291.00	0.89

Appendix 3a: Routing of non-bumping product in wafer fabrication

Step	Equipment	Process Time (Min)	Step	Equipment	Process Time (Min)
1	diff-Clean	11	63	diff-Clean	16
2	diff-1	360	64	diff-1	320
3	Photo	26	65	Photo	29
4	ADI	10	66	ADI	10
5	dry	32	67	dry	32
6	AEI	6	68	AEI	8
7	wet	14	69	wet	14
8	diff-Clean	14	70	CVD_Clean	12
9	diff-1	360	71	CVD	26

10	Photo	32
11	ADI	10
12	dry	36
13	AEI	6
14	wet	15
15	diff-Clean	15
16	diff-1	300
17	Photo	29
18	ADI	10
19	dry	29
20	AEI	10
21	wet	17
22	diff-Clean	20
23	diff-1	320
24	Photo	26
25	ADI	12
26	dry	36
27	AEI	8
28	wet	14
29	diff-Clean	17
30	diff-1	300
31	Photo	32
32	ADI	10
33	dry	32
34	AEI	6
35	wet	15
36	diff-Clean	16
37	diff-1	320
38	Photo	32
39	ADI	12
40	dry	30
41	AEI	8
42	wet	14
43	diff-Clean	18
44	diff-1	360
45	Photo	29
46	ADI	10
47	dry	32
48	AEI	6
49	wet	14
50	diff-Clean	12
51	diff-1	320
52	Photo	32
53	ADI	11
54	dry	36
55	AEI	7
56	wet	15
57	diff-Clean	15
58	diff-1	360
59	Photo	26
60	ADI	12
61	imp1	32
62	wet	15

72	Photo	32
73	ADI	12
74	imp1	26
75	wet	14
76	diff-Clean	17
77	diff-1	320
78	Photo	32
79	ADI	12
80	dry	22
81	AEI	8
82	wet	14
83	PVD_Clean	18
84	PVD	25
85	Photo	26
86	ADI	10
87	dry	32
88	AEI	6
89	wet	14
90	CVD_Clean	15
91	CVD	25
92	Photo	32
93	ADI	12
94	Imp2	32
95	wet	14
96	CVD_Clean	24
97	CVD	29
98	Photo	29
99	ADI	12
100	dry	36
101	AEI	8
102	wet	14
103	PVD_Clean	12
104	PVD	22
105	Photo	32
106	ADI	12
107	dry	26
108	AEI	8
109	wet	14
110	CVD_Clean	10
111	CVD	21
112	Photo	26
113	ADI	10
114	dry	32
115	AEI	6
116	wet	14
117	CVD_Clean	16
118	CVD	25
119	Photo	26
120	ADI	10
121	dry	32
122	AEI	6
123	wet	14

Appendix 3b: Routing of bumping product in wafer fabrication

Step	Equipment	Process Time (Min)
1	diff-Clean	7
2	diff-1	300
3	Photo	32
4	ADI	10
5	dry	32
6	AEI	6
7	wet	14
8	diff-Clean	8
9	diff-1	300
10	Photo	29
11	ADI	10
12	dry	36
13	AEI	6
14	wet	11
15	diff-Clean	12
16	diff-1	360
17	Photo	26
18	ADI	10
19	imp1	26
20	wet	10
21	diff-Clean	12
22	diff-1	320
23	Photo	32
24	ADI	10
25	dry	32
26	AEI	6
27	wet	12
28	diff-Clean	16
29	diff-1	320
30	Photo	29
31	ADI	10
32	dry	32
33	AEI	8
34	wet	14
35	diff-Clean	17
36	diff-1	300
37	Photo	30
38	ADI	12
39	dry	32
40	AEI	8
41	wet	16
42	diff-Clean	11
43	diff-1	250
44	Photo	27
45	ADI	12
46	dry	32
47	AEI	8
48	wet	12
49	diff-Clean	13
50	diff-1	360
51	Photo	34
52	ADI	12
53	dry	32
54	AEI	8
55	wet	16
56	diff-Clean	16
57	diff-1	300
58	Photo	32
59	ADI	12
60	imp1	15
61	wet	12
62	diff-Clean	17
63	diff-1	300
64	Photo	36
65	ADI	12
66	dry	32
67	AEI	8
68	wet	12

69	CVD_Clean	12
70	CVD	32
71	Photo	32
72	ADI	12
73	imp1	12
74	wet	12
75	diff-Clean	12
76	diff-1	250
77	Photo	32
78	ADI	12
79	dry	32
80	AEI	8
81	wet	20
82	CVD_Clean	15
83	CVD	30
84	Photo	26
85	ADI	12
86	dry	32
87	AEI	8
88	wet	15
89	CVD_Clean	14
90	CVD	28
91	Photo	26
92	ADI	12
93	Imp2	32
94	wet	12
95	CVD_Clean	15
96	CVD	26
97	Photo	29
98	ADI	10
99	dry	36
100	AEI	8
101	wet	17
102	CVD_Clean	14
103	CVD	26
104	Photo	32
105	ADI	10
106	dry	36
107	AEI	8
108	wet	15
109	diff-Clean	14
110	diff-1	320
111	Photo	30
112	ADI	12
113	Imp2	29
114	wet	18
115	PVD_Clean	15
116	PVD	29
117	Photo	32
118	ADI	10
119	dry	32
120	AEI	8
121	wet	19
122	CVD_Clean	16
123	CVD	26
124	Photo	29
125	ADI	10
126	dry	36
127	AEI	6
128	wet	14
129	CVD_Clean	15
130	CVD	32
131	Photo	32
132	ADI	10
133	dry	36
134	AEI	9
135	wet	15

Appendix 3c: Routing of bumping product in wafer bumping

Product A

Step	Equipment
1	GP-1
2	GP-2
3	GP-1
4	GP-3
5	GP-4
6	GP-5
7	GP-6
8	GP-7
9	GP-8
10	GP-9
11	GP-8
12	GP-10 (A)
13	GP-11
14	GP-12
15	GP-1
16	GP-13
17	GP-14

Product B

Step	Equipment
1	GP-1
2	GP-2
3	GP-1
4	GP-3
5	GP-4
6	GP-5
7	GP-6
8	GP-7
9	GP-8
10	GP-9
11	GP-8
12	GP-10 (B)
13	GP-11
14	GP-12
15	GP-1
16	GP-9
17	GP-8
18	GP-13
19	GP-14
20	GP-1

Product C

Step	Equipment
1	GP-1
2	GP-2
3	GP-1
4	GP-3
5	GP-4
6	GP-5
7	GP-6
8	GP-7
9	GP-8
10	GP-9
11	GP-8
12	GP-10 (C)
13	GP-11
14	GP-12
15	GP-1
16	GP-8
17	GP-12
18	GP-1
19	GP-8
20	GP-13
21	GP-14
22	GP-1
23	GP-8
24	GP-1

Product D

Step	Equipment
1	GP-1
2	GP-2
3	GP-1
4	GP-3
5	GP-4
6	GP-5
7	GP-6
8	GP-7
9	GP-8
10	GP-9
11	GP-8
12	GP-10 (D)
13	GP-11
14	GP-12
15	GP-1
16	GP-13
17	GP-14

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國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：100 年 08 月 16 日

計畫編號	NSC　99－2221－E－216－029		
計畫名稱	整合式生產策略規劃與管控模式-從晶圓製造到覆晶封裝(I)		
出國人員姓名	杜瑩美	服務機構及職稱	中華大學 工業工程與系統管理學系 教授
會議時間	100 年 8 月 6 日至 100 年 8 月 11 日	會議地點	Lhasa, China
會議名稱	(中文) 資訊與管理科學第十屆國際會議 (英文) The Tenth International Conference on Information and Management Science(IMS2011)		
發表論文題目	(中文) 晶圓製造與覆晶封裝之現場管控模式 (英文) Shop Floor Control Model for Wafer Fabrication and Flip Chip		

一、參加會議經過

The Tenth International Conference on Information and Management Sciences was held in **Lhasa, Tibet, China**. The goals of this Annual Conference of the International Association of Information and Management Sciences are to enhance the global competitiveness of the business enterprises through the applications of research in Information and Management Sciences, and to foster international research collaborations between Asian scholars and scholars in all other parts of the world. In this era of rapid developments of technology, scientific conferences of this type occur in many places at various time frames. In the conference, I presented a paper entitled “Shop Floor Control Model for Wafer Fabrication and Flip Chip” and the topic attracted the attention of attendants because the issue has not been researched a lot in the past. In addition, some other topics about management have been presented and they were all impressed me very much.

二、與會心得

The conference was a forum for researchers and practitioners from all over the world to share their research findings and practical experiences on information and management science issues. This year's conference also combined with another international conference names “The Second International Conference on Uncertainty Theory”. Therefore, the papers regarding to the uncertainty theory were presented in this conference. It enriched the conference very much. A total of 94 papers from different countries around the world were presented in the conference. There are three kinds of presentations in this conference: plenary talks, parallel oral presentation and Best-Paper-Awarding. In the plenary talks, the topic “Integrated Approach to Tool Selection andMachine Loading in Designing and Planning Flexible Manufacturing Cells” by Zahari

Taha impressed me very much. He proposed another view for tool selection and will be a good reference for me. In addition, some presentations such as Yu-Chuan Liu: Buffer Sizing Technique for Fuzzy Critical Chain Scheduling, Dan Ralescu: Statistical Decision under Uncertainty, Lee Young Hae: Supply Chain Management: Present and Future,…etc., are also superb presentations. This conference reaped no little benefit for me.

三、考察參觀活動

During this trip, I made a visit to Professor Zhibin Jiang in ShangHai Chiao Tung University. Professor Jiang is an expert in the production management of semiconductor manufacturing. We exchanged our concepts and opinions in this research fields. Besides, we discussed the differences between Taiwan and mainland China in semiconductor manufacturing. It is a good experience for me. Besides, in Lhasa, the conference arranged all conferee to visit Potala Palace.

四、建議

The 10th International Conference on Information and Management Science was a large conference. As we know that international conference is a good way not only to get new ideas quickly but also to face to face discuss with the authors. Therefore, I suggested that National Science Council and school should review the funding policy and increase the funding amount to encourage and support the teachers and graduate students to attend the international conferences. Besides, I think to hold an international conference is a good way to let everyone in the world to know Taiwan. It is not only to increase the academic position but also to publicize our country. Therefore, it is important to encourage the universities and professor to hold the international conference.

五、攜回資料名稱及內容

- Conference Program :
- The Ninth International Conference on Information and Management Sciences
- The First International Conference of Uncertainty Theory

六、其他

None

The Tenth International Conference
on Information and Management Sciences (IMS2011)
The Second International Conference on Uncertainty Theory (ICUT2011)

August 06-11, 2011, Lhasa, China

May 20, 2011

Shop Floor Control Model for Wafer Fabrication and Flip Chip

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IMS-078

Dear Prof. Ying-Mei Tu,

According to the review reports on your submission, I am very pleased to inform you that your submission has been accepted for presentation at the Tenth International Conference on Information and Management Sciences and the Second International Conference on Uncertainty Theory to be held from August 06-11, 2010 in Lhasa, China. Your contribution will make the conference successful.

The registration form and schedule for the conference are enclosed. There is no page limitation provided that the length is reasonable. It should be noted that at least one of the authors of the paper should register with the conference in order for the paper to be included in the conference proceedings. Please send the registration form and the final version (LATEX or WORD only) of your paper electronically to ims@math.tsinghua.edu.cn before June 20, 2011. To access updated information about the conference, please visit the conference website at http://orsc.edu.cn/ims.

Thank you for your attendance. We look forward to seeing you in Lhasa and sharing your wisdom.

Sincerely yours,

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Shop Floor Control Model for Wafer Fabrication and Flip Chip

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Abstract: Semiconductor manufacturing is a capital and technology intensive high-tech industry with complex processes. As the technology evolution, to satisfy the high pin-count and performance requirements, flip-chip became the predominant technology for chip-to-next level interconnect. Due to yield concern, the tops foundries, such as TSMC & UMC, build their own package factories for flip-chip processes. However, the capacity of flip-chip factory is usually less than fabs' and becomes the bottleneck of all processes. It results in a large number of WIP, long cycle time and overdue orders and comes into being the disaster of foundry.
In this study, a shop floor control model for wafer fabrication and flip-chip factory will be developed. It includes job release policy and lot priority adjustment rule of wafer fab. Due to the variability of package technique and demand, a shop floor control model will be developed to solve current production planning and control issues. A dynamic lot priority adjustment rule will be established to apply to fab. This rule will be based on the WIP level of flip chip to dynamically adjust the lot priority in wafer fabrication stage. Therefore, the dynamic buffer management will be applied to control WIPs of fab. In this work, the lower bound and upper bound of WIP in front of constraint machine will be set and to divide the WIP level into three zones, red, yellow and green zone. When WIP level falls into red zone (less than lower bound), lot priority in wafer fabrication stage should be set higher. On the contrary, if WIP level falls into green zone (more than upper bound), lot priority can be set lower. Furthermore, DBR scheduling concept will be applied to the wafer release plan for flip-chip factory. According to the pace of the constraint machine to release wafer, it can make sure to maximize the factory throughput and to keep the WIP lower. Hence, based on these two controls, the flow will be more smooth and efficient both on wafer fabrication and flip-chip factory.

Keywords: Wafer fabrication, Flip-chip package, Shop floor control, Dynamic buffer management, DBR scheduling

I. Introduction

Recently, the market needs to drive consumer electronic products to be smaller, faster and higher functionality. The trend in microelectronic packaging technology is toward miniaturization and high performance. In order to keep the competition, IC companies are forced to introduce advance technology no matter in wafer fabrication, probe, testing or assembly. However, the new generation technology always becomes the bottleneck of the whole process when an advanced technology is first introduced. Due to the uncertainty of future demand, to speed the technology migration rate or just keep in watch will be a dilemma when the capacity of new technology shortage happens. This phenomenon is also occurred in the flip chip process. As the technology evolution, to satisfy the high pin-count and performance requirements, flip-chip became the predominant technology for chip-to-next level interconnect. Flip chip bonding was first introduced by IBM in 1964. It was called controlled collapse chip connection (C4) by IBM, in which the flow of the solder bump during soldering is controlled by the die solder bump volume, area of the solder wet-table pad on the substrate, the die weight and the solder surface tension[14]. Due to yield concern, the tops foundries, such as TSMC & UMC, build their own package factories for flip-chip processes. Under this production strategy, the products in foundry can be separated into two parts, non-bumping process and bumping process. Nonetheless, the capacity of flip-chip factory is usually less than fabs' and becomes the bottleneck of all stages. It results in a large number of WIP, long cycle time and overdue orders and comes into being the disaster of foundry. The most effective solution for the issue is to increase the capacity of flip chip factory. As well known, the capacity plan is a long term plan. It means the capacity can not be increased within a short time. Especially, when the market demand is instinct with uncertainty, it is hard to decide to increase capacity. Under this situation, a suitable shop floor control model for wafer fabrication and flip-chip factory will be the best way to relieve the disaster of foundry.
In the past studies, all shop floor control models are designed for only one kind of factory, especially for fab [1], [8], [11]. As we know, wafer fabrication is a capital intensive industry. Therefore, to fully utilize the production resources to get the maximum output and shortening cycle time are the major targets of all fabs [4], [5], [10]. Nevertheless, although the fabs perform well, the bumping products are still pilled in the flip chip factory. From the

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company management point of view, this kind of orders will take a long cycle times or even be overdue. Hence, a shop floor control model links with wafer fabrication and flip chip factory is needed. It should manage not only fab production but also flip chip portion.

Accordingly, an integrated shop floor control model is developed in this work. It includes job release policy and dynamic lot priority adjustment rules. Both release policy and priority rules are based on the bottleneck machine (platting equipment) to set the production smoothness f the whole processes. Under this control, both fab and flip chip factory can get the better performances. This paper was structured as follows. In the next section, the job release policy and dynamic lot priority adjustment rules are proposed. In section 3, a numerical example is presented to demonstrate this control model. Finally, the summary and future researches are included in Section 4.

II. Integrated Shop Floor Control Model (isfc)

Generally, wafer fabrication and flip chip factory are two separated factories and managed by different teams and rules. However, the flip chip factory should take the result of fab. If the production management of fab focuses on their own factory only, the chip flip factory will suffer the variability of fab's output. Therefore, an integrated shop floor control model to link with fab and flip chip factory is very important for the whole performance. In this model, there are two parts of rules, including job release policy and lot priority adjustment rule of wafer fab. Although these rules all will be acted in fab, the indicator will be the bottleneck of whole processes. In other word, it will be the plating equipment in this model. The details are described as follows.

A. NOTATION

The following terminology is required for the capacity support control model.

$\lambda_{bumping}$: Arrival rate of bumping products in fab

$\mu_{bottleneck}$: Service rate of plating workstation in flip chip factory

$\tau_{bottleneck}$: Service time of plating workstation in flip chip factory

$A_{bottleneck}$: Availability of plating workstation in flip chip factory

M : Number of bottleneck machines

s : Lower bound of WIP level

ECL_i : Expected capacity loss of feeder machines of bottleneck machine

$ECL_{bottleneck}$: Expected capacity loss of bottleneck machine

PT_j : Processing time of upstream machine

$PT_{bottleneck}$: Processing time of bottleneck machine

$MTTR_i$: Mean time to repair(MTTR) of Feeder machines

S : Upper bound of WIP level

EQ : Expected queue length of bottleneck machine

$\rho_{bottleneck}$: The utilization goal of bottleneck machine

ω : allowance

B. RELEASE POLICY

Based on TOC (Theory of Constraints) concept, it reveals that the system performance is decided by system constraint (i.e. the bottleneck of the production system) and all non-constrains should subordinate the constraint [6], [7]. Generally, the bottleneck of flip chip factory is the plating workstations. Hence, the wafer release tempo should be based on the production rate of plating workstation [9], [13]. However, as mentioned above, the release of flip chip factory comes from the output of fab. If the factor of flip chip factory's constraint can't be taken into account to the release policy of fab, any production planning can't be effective. Therefore, the release rate of bumping products to the fab should be based on the production rate of plating workstation. Basically, the major factor affecting the production rate is the processing time. In addition, the capacity loss, for example machines breakdown, will also impact the production rate. Hence, the production rate of bottleneck should be modified by the availability of workstation. Based on these concepts, the production rate of plating workstation can be identified as the following equation.

$$\lambda_{bumping} = \mu_{bottleneck} = \frac{M}{(\frac{\tau_{bottleneck}}{A_{bottleneck}})} \quad (1)$$

It can be made a conclusion that the bumping products have to be released by the same rate as the service rate of the bottleneck of flip chip factory. As we know, there is another kind of products processed in fab and the capacity of fab is more than flip chip factory. Therefore, the actual arrival rate in fab will larger than the arrival rate of bumping products. The relation can be described as follows.

$$\lambda_{fab} = \lambda_{bumping} + \lambda_{non-bumping} \quad (2)$$

C. DYNAMIC LOT PRIORITY ADJUSTMENT RULE

The production environment is full of uncertainty and unpredictable events, such as machine breakdown, material shortage, staffs' leaving,…etc[11]. Although the release policy is perfect, the production schedule is still disturbed by the unpredictable events. Finally, the execution results are far away from the plan. Shop floor control is the best way to amend this result. Same as the release policy, the shop floor control rules should be also taken the status of flip chip factory into account and have to adjust the production rate of bumping product dynamically in wafer fabrication stage. In order to avoiding the starvation of bottleneck machine and lengthening the waiting time of bumping products in flip chip factory, the concepts of buffer management in TOC (Theory of Constraints) are applied. The WIP level of bottleneck machine is divided into three zones by lower bound and upper bound, names red, yellow and green zone. When the WIP level is falling into the red zone, it means that the WIP level is too low to protect the bottleneck machine from starvation. Hence, the priority of bumping products should be higher to push the WIP into flip chip factory quickly. On the contrary, if the WIP level is falling into the green zone, it stands for the WIP level is too high. Too many WIPs waiting in front of bottleneck machine will increase the cycle time of products [2], [4], [5], [12]. Therefore, the priority of bumping products should be lower down in wafer fabrication stage to decrease the arrival rate of bumping products into flip chip factory.

Based the description above, the critical point of this dynamic lot priority adjustment rule is how to define the lower bound and upper bound of WIP level. The purpose of lower bound is to avoid the starvation of bottleneck machine. The major cause of machine starvation is the capacity loss of feeder machines. Under this situation, the lower bound will be the amount of WIP to cover the capacity loss of feeder machines. Besides, although the priority of bumping products are heightening in wafer fabrication stage and make them to flow into flip chip factory quickly, the bumping products still should take time to arrive the bottleneck machine. Therefore, the time from the first workstation to the bottleneck has to take into consideration. Accordingly, the lower bound of bottleneck can be described as the following equations.

$$s = (\sum_{i=1}^{n} ECL_i - ECL_{bottleneck}) + \frac{\sum_{j=1}^{m} PT_j}{PT_{bottleneck}} \quad (3)$$

$$ECL_i = MTTR_i \times \mu_i \times (1 - A_i) \quad (4)$$

The major purpose of the upper bound is to prevent the long cycle time of products. The queuing theory is applied to the formulation. Based on the queuing theory, waiting time of products is decided by the utilization of equipment. When the managers set the goal of cycle time of products, the utilization of equipment can be calculated. The expected queue length can also be derived based on the utilization of equipment. Because the expected queue length is just an average number, the allowance is put into the upper bound equation and expresses as follows.

$$S = EQ(\rho_{bottleneck}, M) \times \omega \quad (5)$$

$$EQ(\rho_{bottleneck}, M) = \frac{P \times \left(\frac{\lambda}{\mu}\right) \times \rho}{M! \times (1-\rho)^2} \quad (6)$$

$$P = ((\sum_{n=0}^{M-1} (\frac{1}{n!} \times \left[\frac{\lambda}{\mu}\right]^n)) + \frac{1}{M!} \times \left[\frac{\lambda}{\mu}\right]^{Mn} \times \frac{M \times \mu}{M \times \mu - \lambda})^{-1} \quad (7)$$

$$\rho = \frac{\lambda}{M \times \mu} \quad (8)$$

III. **Numerical Example**

Appendix 1, 2 and 3 show illustrate the preliminary data concerning the example, including information about the master production schedule (MPS), the machines and the routing of products. The measure unit of releasing batch into factory is "lot". A lot includes 25 wafers. The release policy is of uniform distribution. A wafer factory can normally be divided into seven areas, with more than one machine in each. Machines in the same area perform the same functions. The processing time is defined by recipe in wafer fabrication, however, it is defined by equipment in flip chip factory.

This example assumes that the equipment of GP10 (Plating equipment) is the bottleneck machine in flip chip factory. Therefore, the release rate of bumping products in wafer fabrication is as follows.

Based on equipment list of wafer bumping, it shows that the WPH (Wafer Per Hour) of GP10 by product are as follows.

Product	Service Time(hrs)
A	(3.316+3.125+6.812)/3=4.418
B	(6.812+4*4.587)/5=5.032
C	(6.812+4*4.587)/5=5.032
D	4.587

$$\tau_{GP10} = \frac{540}{1141} \times 4.418 + \frac{420}{1141} \times 5.032 + \frac{200}{1141} \times 5.032 + \frac{1}{1141} \times 4.587 = 4.752$$

$$A_{GP10} = (0.91 + 0.94 + 0.93 + 0.93 + 0.91 + 0.9 + 0.93 + 0.93)/8 = 0.92$$

$$\lambda_{bumping} = \mu_{GP10} = \frac{8}{(\frac{4.752}{0.92})} = 1.55(lot/hour)$$

Based on the equation 3 and 5, the lower bound and upper bound of GP10's WIP level can be derived as follows.
Assume ω=1.1
Average Process Time of equipment in flip chip factory:

Equipment	Average Process Time (Hrs)
GP1	0.246
GP2	1.041
GP3	1.520
GP4	0.650
GP5	0.840
GP6	1.220
GP7	1.294
GP8	0.703
GP9	1.420
GP10	4.752
GP11	1.826
GP12	1.021
GP13	1.125
GP14	2.013

The expected capacity loss of feeder machines :

$$\sum_{i=1}^{n} ECL_i = ECL_{GP8-1} + ECL_{GP8-2} + ECL_{GP8-3} + ECL_{GP8-4}$$
$$= 110.4*1/0.703*(1-0.9) + 151.8*1/0.703*(1-0.9) + 100.2*1/0.703*(1-0.9) + 156.6*1/0.703*(1-0.9) = 73.8$$

$$ELC_{bottleneck} = 273*1/3.316*(1-0.91) + 301.8*1/3.125*(1-0.91) + 285.6*1/6.812*(1-0.94) + 309*1/4.587*(1-0.93) + 268.2*1/4.587*(1-0.93) + 292.2*1/4.587*(1-0.93) + 300.6*1/4.587*(1-0.93) + 745.8*1/4.587*(1-0.90) = 52.73$$

The time from the first workstation to the bottleneck:

$$\sum_{j=1}^{m} PT_j = PT_{GP-1} + PT_{GP-2} + PT_{GP-1} + PT_{GP-3} + PT_{GP-4} + PT_{GP-5} + PT_{GP-6} + PT_{GP-7} + PT_{GP-8} + PT_{GP-9} + PT_{GP-8} = 9.86(Hrs)$$

Therefore, the lower bound can be defined as follows.

$$s = 73.8 - 52.73 + 9.86/4.752 = 23.15 \approx 24(lots)$$

$$P = ((\sum_{n=0}^{7} \frac{1}{n!} \times \left[\frac{1.5178}{0.1936}\right]^n) + \frac{1}{8!} \times \left[\frac{1.5178}{0.1936}\right]^8 \times \frac{8 \times 0.1936}{8 \times 0.1936 - 1.5178})^{-1} = 0.000053$$

$$\rho = \frac{1.5178}{8 \times 0.1936} = 0.98$$

$$EQ(\rho_{bottleneck}, M) = \frac{0.000053 \times \left(\frac{1.578}{0.1936}\right) \times 0.98}{8! \times (1-0.99)^2} = 45.9$$

$$S = EQ(\rho_{bottleneck}, M) \times \omega = 45.9 \times 1.1 = 50.49 \approx 51(lots)$$

IV Conclusion

In this work, an integrated shop floor control model between wafer fabrication and flip chip is established to enhance the whole production performance. There were two control rules are developed, wafer release policy and dynamic lot priority adjustment rules. Both of them are based on the bottleneck of whole production line to manage the production tempo. Through these two control rules, the production performances of wafer fabrication and flip chip factory will be improved.
Regarding to the future works, there are two points can be considered. The first one is the effect of deviation of wafer release on the production performance. Actually, the studies of release policy in most of researches focus the mean of arrival rate. However, the sources of performance variation come from the deviation of control factors. Therefore, the sensitivity of deviation of arrival rate is

worth studying. Besides, the arrival pattern is another factor which will affect on the production performance. Although the arrival pattern can not be well controlled in the real life, it can be studied how the performance is affected. Finally, this result can be used to adjust the shop floor status.

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Appendices

Appendix 1: Master Production Schedule

Wafer fabrication

Product	Demand(lot/month)
Non-bumping	2282
bumping	1093

Wafer bumping

Product	Demand(lot/month)
A	520
B	420
C	200
D	1

Appendix 2: Machine information
Wafer fabrication

Equipment	M/C Qty	MTTR (Hr)	MTBF (Hr)	Availability
ADI	19	1.5	48.50	0.97
AEI	10	1	49.00	0.98
cvd-1	14	3	72.00	0.96
cvd-clean	8	1	49.00	0.98
diff-1	55	5	95.00	0.95
diff-clean	15	1	49.00	0.98
dry-1	46	2.5	25.28	0.91
imp-1	6	2	20.22	0.91
imp-2	4	1.5	48.50	0.97
photo	49	2	38.00	0.95
pvd-1	4	1	49.00	0.98
pvd-clean	3	0.5	49.50	0.99
wet-1	25	2.5	39.17	0.94

Wafer bumping

Equipment	M/C Qty	Process Time (Hrs)	MTTR(Hrs)	AVAIL(%)
GP-1-1	1	0.246	70.20	0.92
GP-1-2	1	0.246	61.80	0.92
GP-2 -1	1	1.111	249.00	0.57
GP-2 -2	1	1.045	208.20	0.59
GP-2 -3	1	0.968	211.20	0.57
GP-3 -1	1	1.644	65.40	0.82
GP-3 -2	1	1.535	66.00	0.82
GP-3 -3	1	1.382	64.80	0.82
GP-4 -1	1	0.767	56.40	0.85
GP-4 -2	1	0.533	57.00	0.85
GP-5 -1	1	0.966	82.20	0.87
GP-5 -2	1	0.714	59.40	0.90
GP-6 -1	1	1.268	55.80	0.90
GP-6 -2	1	1.268	88.80	0.90
GP-6 -3	1	1.125	166.80	0.90
GP-7-1	1	1.294	225.60	0.90
GP-7-2	1	1.294	243.00	0.90
GP-7-3	1	1.294	191.40	0.90
GP-8-1	1	0.703	110.40	0.90
GP-8-2	1	0.703	151.80	0.90
GP-8-3	1	0.703	100.20	0.90
GP-8-4	1	0.703	156.60	0.90
GP-9-1	1	1.420	0.00	0.94
GP-9-2	1	1.420	0.00	0.94
GP-9-3	1	1.420	74.40	0.94
GP-9-4	1	1.420	140.40	0.94
GP-9-5	1	1.420	56.40	0.94
GP-10 (A) -1	1	3.316	273.00	0.91
GP-10 (A) -2	1	3.125	301.80	0.91
GP-10 (A/ B/ C)	1	6.812	285.60	0.94
GP-10 (B/ C)-1	1	4.587	309.00	0.93
GP-10 (B/ C)-2	1	4.587	268.20	0.93
GP-10 (B/ C)-3	1	4.587	292.20	0.93
GP-10 (B/ C)-4	1	4.587	300.60	0.93
GP-10 (D)	1	4.587	745.80	0.90
GP-11 -1	1	1.561	75.60	0.85
GP-11 -2	1	1.561	227.40	0.85
GP-11 -3	1	1.561	127.20	0.85
GP-11 -4	1	2.621	137.40	0.85
GP-12-1	1	1.021	195.00	0.86
GP-12-2	1	1.021	151.20	0.86
GP-12-3	1	1.021	333.00	0.86
GP-13-1	1	1.125	253.20	0.61
GP-13-1	1	1.125	277.20	0.61
GP-13-1	1	1.125	253.80	0.61
GP-14-1	1	2.013	250.20	0.89
GP-14-2	1	2.013	225.00	0.89
GP-14-3	1	2.013	319.20	0.89
GP-14-4	1	2.013	291.00	0.89

Appendix 3a: Routing of non-bumping product in wafer fabrication

Step	Equipment	Process Time (Min)	Step	Equipment	Process Time (Min)
1	diff-Clean	11	63	diff-Clean	16
2	diff-1	360	64	diff-1	320
3	Photo	26	65	Photo	29
4	ADI	10	66	ADI	10
5	dry	32	67	dry	32
6	AEI	6	68	AEI	8
7	wet	14	69	wet	14
8	diff-Clean	14	70	CVD_Clean	12
9	diff-1	360	71	CVD	26

10	Photo	32
11	ADI	10
12	dry	36
13	AEI	6
14	wet	15
15	diff-Clean	15
16	diff-1	300
17	Photo	29
18	ADI	10
19	dry	29
20	AEI	10
21	wet	17
22	diff-Clean	20
23	diff-1	320
24	Photo	26
25	ADI	12
26	dry	36
27	AEI	8
28	wet	14
29	diff-Clean	17
30	diff-1	300
31	Photo	32
32	ADI	10
33	dry	32
34	AEI	6
35	wet	15
36	diff-Clean	16
37	diff-1	320
38	Photo	32
39	ADI	12
40	dry	30
41	AEI	8
42	wet	14
43	diff-Clean	18
44	diff-1	360
45	Photo	29
46	ADI	10
47	dry	32
48	AEI	6
49	wet	14
50	diff-Clean	12
51	diff-1	320
52	Photo	32
53	ADI	11
54	dry	36
55	AEI	7
56	wet	15
57	diff-Clean	15
58	diff-1	360
59	Photo	26
60	ADI	12
61	imp1	32
62	wet	15

72	Photo	32
73	ADI	12
74	imp1	26
75	wet	14
76	diff-Clean	17
77	diff-1	320
78	Photo	32
79	ADI	12
80	dry	22
81	AEI	8
82	wet	14
83	PVD_Clean	18
84	PVD	25
85	Photo	26
86	ADI	10
87	dry	32
88	AEI	6
89	wet	14
90	CVD_Clean	15
91	CVD	25
92	Photo	32
93	ADI	12
94	Imp2	32
95	wet	14
96	CVD_Clean	24
97	CVD	29
98	Photo	29
99	ADI	12
100	dry	36
101	AEI	8
102	wet	14
103	PVD_Clean	12
104	PVD	22
105	Photo	32
106	ADI	12
107	dry	26
108	AEI	8
109	wet	14
110	CVD_Clean	10
111	CVD	21
112	Photo	26
113	ADI	10
114	dry	32
115	AEI	6
116	wet	14
117	CVD_Clean	16
118	CVD	25
119	Photo	26
120	ADI	10
121	dry	32
122	AEI	6
123	wet	14

Appendix 3b: Routing of bumping product in wafer fabrication

Step	Equipment	Process Time (Min)
1	diff-Clean	7
2	diff-1	300
3	Photo	32
4	ADI	10
5	dry	32
6	AEI	6
7	wet	14
8	diff-Clean	8
9	diff-1	300
10	Photo	29
11	ADI	10
12	dry	36
13	AEI	6
14	wet	11
15	diff-Clean	12
16	diff-1	360
17	Photo	26
18	ADI	10
19	imp1	26
20	wet	10
21	diff-Clean	12
22	diff-1	320
23	Photo	32
24	ADI	10
25	dry	32
26	AEI	6
27	wet	12
28	diff-Clean	16
29	diff-1	320
30	Photo	29
31	ADI	10
32	dry	32
33	AEI	8
34	wet	14
35	diff-Clean	17
36	diff-1	300
37	Photo	30
38	ADI	12
39	dry	32
40	AEI	8
41	wet	16
42	diff-Clean	11
43	diff-1	250
44	Photo	27
45	ADI	12
46	dry	32
47	AEI	8
48	wet	12
49	diff-Clean	13
50	diff-1	360
51	Photo	34
52	ADI	12
53	dry	32
54	AEI	8
55	wet	16
56	diff-Clean	16
57	diff-1	300
58	Photo	32
59	ADI	12
60	imp1	15
61	wet	12
62	diff-Clean	17
63	diff-1	300
64	Photo	36
65	ADI	12
66	dry	32
67	AEI	8
68	wet	12

69	CVD_Clean	12
70	CVD	32
71	Photo	32
72	ADI	12
73	imp1	12
74	wet	12
75	diff-Clean	12
76	diff-1	250
77	Photo	32
78	ADI	12
79	dry	32
80	AEI	8
81	wet	20
82	CVD_Clean	15
83	CVD	30
84	Photo	26
85	ADI	12
86	dry	32
87	AEI	8
88	wet	15
89	CVD_Clean	14
90	CVD	28
91	Photo	26
92	ADI	12
93	Imp2	32
94	wet	12
95	CVD_Clean	15
96	CVD	26
97	Photo	29
98	ADI	10
99	dry	36
100	AEI	8
101	wet	17
102	CVD_Clean	14
103	CVD	26
104	Photo	32
105	ADI	10
106	dry	36
107	AEI	8
108	wet	15
109	diff-Clean	14
110	diff-1	320
111	Photo	30
112	ADI	12
113	Imp2	29
114	wet	18
115	PVD_Clean	15
116	PVD	29
117	Photo	32
118	ADI	10
119	dry	32
120	AEI	8
121	wet	19
122	CVD_Clean	16
123	CVD	26
124	Photo	29
125	ADI	10
126	dry	36
127	AEI	6
128	wet	14
129	CVD_Clean	15
130	CVD	32
131	Photo	32
132	ADI	10
133	dry	36
134	AEI	9
135	wet	15

Appendix 3c: Routing of bumping product in wafer bumping

Product A

Step	Equipment
1	GP-1
2	GP-2
3	GP-1
4	GP-3
5	GP-4
6	GP-5
7	GP-6
8	GP-7
9	GP-8
10	GP-9
11	GP-8
12	GP-10 (A)
13	GP-11
14	GP-12
15	GP-1
16	GP-13
17	GP-14

Product B

Step	Equipment
1	GP-1
2	GP-2
3	GP-1
4	GP-3
5	GP-4
6	GP-5
7	GP-6
8	GP-7
9	GP-8
10	GP-9
11	GP-8
12	GP-10 (B)
13	GP-11
14	GP-12
15	GP-1
16	GP-9
17	GP-8
18	GP-13
19	GP-14
20	GP-1

Product C

Step	Equipment
1	GP-1
2	GP-2
3	GP-1
4	GP-3
5	GP-4
6	GP-5
7	GP-6
8	GP-7
9	GP-8
10	GP-9
11	GP-8
12	GP-10 (C)
13	GP-11
14	GP-12
15	GP-1
16	GP-8
17	GP-12
18	GP-1
19	GP-8
20	GP-13
21	GP-14
22	GP-1
23	GP-8
24	GP-1

Product D

Step	Equipment
1	GP-1
2	GP-2
3	GP-1
4	GP-3
5	GP-4
6	GP-5
7	GP-6
8	GP-7
9	GP-8
10	GP-9
11	GP-8
12	GP-10 (D)
13	GP-11
14	GP-12
15	GP-1
16	GP-13
17	GP-14

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國科會補助計畫衍生研發成果推廣資料表

日期:2011/10/03

國科會補助計畫	計畫名稱: 整合式生產策略規劃與管控模式-從晶圓製造到覆晶封裝(I)
	計畫主持人: 杜瑩美
	計畫編號: 99-2221-E-216-029- 學門領域: 生產系統規劃與管制

無研發成果推廣資料

99 年度專題研究計畫研究成果彙整表

計畫主持人：杜瑩美	計畫編號：99-2221-E-216-029-
計畫名稱：整合式生產策略規劃與管控模式-從晶圓製造到覆晶封裝(I)	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	1	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	0	0	100%	人次	
		博士生	2	2	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	1	1	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	無

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：□已發表 □未發表之文稿 ■撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：(以 100 字為限)

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）(以 500 字為限)

由於製程世代的轉換對於半導體產業的永續存在著一定程度影響，如何適時安排新製程的導入，使得在轉換時公司依舊保持著一定的競爭優勢，快速的反應需求的變動，將生產能力調整到最適宜的，不至於因新製程的導入而引發更多的問題，實為未來研究值得探討之方向。

就本質而論，本計畫之研究成果同時具有實務及學術價值。在實務方面，本計畫之成果提供晶圓廠對於覆晶封裝之產能現場管控方式能有所憑藉；在學術上，本研究提供一套以緩衝管理理論為基礎，應用於半導體廠中之前後段晶圓製造製程現場管控之概念。此外，本研究亦已將研究成果發表於國際學術研討會之中。

本研究之主要成果分述如下：

1. 連結晶圓製造廠前段與後段製程之管理與規劃，提供一個有系統之解決邏輯的投料法則與現場管控模式。

2. 發展瓶頸機台加工節奏之估算模式，以制訂後段製程之投料節奏，最後再加入所有產品型態影響之後，完成前段製程之投料決策模式。

3. 從 TOC 當中緩衝管理的角度思考，針對後段晶圓製造覆晶封裝製程生產步調，提出一套有效且合理之前段製程動態調整在製品之加工優先現場管控模式。

4. 利用 eM-Plant 7.0 呈現與建構前後段晶圓製造之製程過程與特性，以提供後續相關之研究平台。