Capacity planning with sequential two-level of time constraints in the back-end of wafer fabrication

杜瑩美,陳欣男
Industrial Engineering and System Management
Management
amytu@chu.edu.tw

Abstract

Time constraint is a queue-time boundary which is set between particular sequential operations to ensure final product yield. These time boundaries, named “sequential time constraints,” can be found in a series of operations in the back-end of wafer fabrications. Wafers exceeding the time constraints are traced through the fabrication process but generally undergo the remaining processes. Nonetheless, it is a waste of capacity to continue processing wafers with unacceptable yield. Unfortunately, these unacceptable wafers cannot be identified before wafer acceptance test in current control policy.

This work proposes a control rule of two-level time constraints, with capacity planning methodology under this rule. Wafers exceeding the lower time constraints will be treated as normal wafers; however, once wafers exceed the upper time constraints, they will be scrapped immediately. In the capacity planning model, a GI/G/m queuing network is applied to determine the required numbers of machines. By pre-setting target yields, the rates of wafers being marked or scrapped can be controlled. Furthermore, a novel scheme -- regarding machine failures as irregular customers -- is introduced to describe the effect of service interruptions. The results support that the proposed control rule and capacity planning model can more effectively resolve the issues of sequential time constraints. Moreover, the analysis results indicate that the current capacity expansion policy of the semiconductor industry should be re-examined.

Keyword：capacity planning; sequential time constraints; queuing networks; wafer fabrications