CMOS Current-Mode Companding Multiplier/Divider and Its Nth-Root

林國珍,鄭智仁,陳竹一
Microelectronics Engineering
Engineering
kuojenlin@chu.edu.tw

Abstract

A CMOS current-mode companding multiplier/divider composed of three compact logarithm
circuits and one compact exponential circuit is proposed. Approaches for constructing the logarithm circuits and
the exponential circuit are based on second-order Taylor series approximations. By gathering the three logarithm
results and passing through the exponential circuit, we can obtain the result of zp(xq/yr). The circuitry complexity
is very low with only 12 transistors. The simulation results indicate that the relative errors of the proposed circuit
are small for small (p+q+r).

Keyword：Taylor series approximation, Current-mode multiplier/divider, Companding, Log-domain