A ROM-Less Direct Digital Frequency Synthesizer Based on a Scaling-free CORDIC algorithm

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Abstract

A ROM-less direct digital frequency synthesizer (DDFS) based on the modified scaling-free CORDIC algorithm is presented. Compared to the DDFS used conventional CORDIC, this algorithm reduces a half of iteration by using modified scaling-free CORDIC on average. The corresponding design procedure with error, performance and hardware analysis has been given that leads to an optimized solution. The algorithm and its applications are implemented on FPGA (field programmable gate array) by using Verilog codes. The worse case spurious-free dynamic range (SFDR) is better than 80.5 dBc.

Keyword：DDFS; scaling-free CORDIC algorithm; SFDR;