Design and Optimization of Direct Digital Frequency Synthesizer

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Abstract

Scaling-free CORDIC (COordinate Rotation DIgital Computer) is one of the famous CORDIC implementations with advantages of speed and area. In this paper, a novel direct digital frequency synthesizer (DDFS) based on scaling-free CORDIC is presented. The proposed multiplier-less architecture with small ROM and pipeline data path has advantages of high data rate, high precision, high performance, and less hardware cost. The design procedure with performance and hardware analysis for optimization has also been given. It is verified by Matlab® simulations and then implemented with FPGA (field programmable gate array) by Verilog®

. The spurious-free dynamic range (SFDR) is over 86.85 dBc, and the signal-to-noise ratio (SNR) is more than 81.12 dB. The scaling-free CORDIC based architecture is suitable for VLSI implementations for the DDFS applications in terms of hardware cost, power consumption, SNR, and SFDR.

Keyword：DDFS, scaling-free CORDIC, SFDR, SNR, FPGA, VLSI.