Simultaneous Escape Routing Based on Routability-Driven Net Ordering

顏金泰,宋東彥,陳志瑋
Computer Science & Information Engineering
Computer Science and Informatics
yan@chu.edu.tw

Abstract

In this paper, given a set of n escape nets between an array of pxq pins and an array of rxs pins, firstly, a routability-driven net order between two given pin arrays is determined for simultaneous escape routing. Furthermore, based on ordered escape routing for two pin arrays, an efficient approach is proposed to solve the routing problem for simultaneous escape routing. Compared with Kong's flow-based approach[11] for three tested examples, the experimental results show that our proposed approach achieves 100% routability for the tested examples and reduces the CPU time by 54.1% on the average.

Keyword：PCB design, Escape routing, Single-layer routing