Utilization of Multi-Bit Flip-Flops for Clock Power Reduction

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Abstract

Utilization of multi-bit flip-flops in a synchronous design has been becoming a significant methodology for clock power reduction. However, some published approaches are usually based on the assumption that the bit number of the flip-flops is continuous or the number of the available flip-flops is infinite in a cell library. Under the physical limitation of the flip-flop cells in a real cell library, the bit number of the flip-flops is discrete and the number of the available flip-flops is finite. In this paper, given a synchronous system with a set of 1-bit flip-flops in a placement plane, the timing constraints of the associated signals in the flip-flops and the available flip-flops in a real cell library, based on the bit number of the available multi-bit flip-flops in the given cell library, an optimal approach is proposed to obtain the maximum power-saving result by merging 1-bit flip-flops into the available flip-flops. Compared with the original synchronous designs using 1-bit flip-flops, the experimental results show that our proposed approach reduces 38.4% of the flip-flop area and saves 24.9% of the clock power to maintain the synchronous property on the average for five tested examples in reasonable CPU time.

Keyword：multi-bit flip-flop, Clocl power