Assignment of Adjustable Delay Buffers for Clock Skew Minimization in Multi-Voltage Mode Designs

顏金泰,陳志瑋
Computer Science & Information Engineering
Computer Science and Informatics
yan@chu.edu.tw

Abstract

It is well known that clock skew minimization becomes critical in high-performance VLSI designs. In this paper, the assignment of adjustable delay buffers(ADBs) is applied to minimize the clock skew in a buffered clock tree in a multi-voltage mode design. Given a buffered clock tree, based on the assignment flexibility of the delay value on an ADB, bottom-up ADB assignment is firstly proposed to insert ADBs to minimize the clock skew by assigning the delay values of the inserted ADBs for each power mode. Furthermore, bottom-up ADB elimination is proposed to eliminate the redundant ADBs to minimize the number of the inserted ADBs in a multi-voltage mode design while maintaining the minimized clock skew. Compared with Su's heuristic algorithm and Lim's optimal algorithm, the experimental results show that our proposed algorithm uses less CPU time to reduces 9.3% of the used ADBs and 1.3%~1.6% of the average latency on the average, respectively.

Keyword：ADB, Clock skew