Routability-Driven Flip-Flop Merging Process for Clock Power Reduction

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Abstract

The concept of merging some 1-bit flip-flops into a multi-bit flip-flop is applied to reduce dynamic clock power and decrease the total flip-flop area in a synchronous design. To acquire these advantages, the design must be guaranteed to satisfy certain physical constraints in the merging process. In this paper, given a set of 1-bit flip-flops with the input and output timing constraints, the area constraint inside any partitioned bin and the capacity constraint on any bin edge in a placement plane, an efficient routability-driven approach is proposed to merge 1-bit flip-flops into some multi-bit flip-flops for clock power reduction. The experimental results show that our proposed approach reduces 37.4% of the flip-flop area to maintain the synchronous design and saves 24.82% of the clock power for five examples in reasonable CPU time on the average.

Keyword：Low-power design, Flip-flop merging, Routability