# Low-Cost Low-Power Bypassing-Based Multiplier Design

顏金泰,陳志瑋
Computer Science & Information Engineering
Computer Science and Informatics
yan@chu.edu.tw

## Abstract

Based on the simplification of the incremental adders instead of full adders in an array multiplier, a low-cost low-power bypassing-based multiplier is proposed. Compared with row-bypassing multiplier[7], column-bypassing multiplier[8] and 2-dimensional bypassing-based multiplier[9-10] for 20 tested examples, the experimental results show that our proposed low-cost low-power multiplier saves 15.1% of transistors and reduces 29.6% of the power dissipation on the average for 4x4, 8x8 and 16x16 multipliers.

Keyword：Low power, Multiplier