# Efficient selection strategies towards processor reordering techniques for improving data locality in heterogeneous clusters

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## Abstract

Grid architecture integrates geographically distributed nodes to manage
and provide resources to execute scientific applications. For data locality, applications
with different computational phases require data redistribution for realignment.
The tradeoff between high efficiency computation and communication cost of data
redistribution accompanies. This paper introduces a research model and two methods
to derive new lists of processor logical id according to the characteristics of heterogeneous
network. Both methods provide choices of more low-cost communication schedules in grid. The simulations show both proposed methods yield outstanding
performance in grid.

Keyword：Selection strategy ‧ Processor reordering