Routability-Constrained Multi-Bit Flip-Flop Construction for Clock Power Reduction

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Abstract

Reducing the power consumption of a clock network is always one of critical issues in designing a high performance design. The concept of multi-bit flip-flop construction has been introduced by recent studies and shown the benefits of reducing clock power and decreasing the total flip-flop area in a synchronous design. However, all the works are not considering the routability issue which caused by merging multiple 1-bit flip-flops into multi-bit flip-flops. In this paper, given a set of 1-bit flip-flops with the input and output timing constraints, the area constraint inside any partitioned bin and the capacity constraint on any bin edge in a placement plane, an efficient routability-constrained approach is proposed to merge 1-bit flip-flops into some multi-bit flip-flops for clock power reduction. The experimental results show that our proposed approach reduces 37.4% of the flip-flop area to maintain the synchronous design and saves 24.82% of the clock power for five examples in reasonable CPU time on the average.

Keyword：Multi-bit flip-flop, Clock power